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DEVELOPMENT AND EVALUATION OF A SHIPBOARD INTEGRATED NAVIGATION AND DISPLAY SYSTEM

Prepared for
Transportation Development Centre
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by
OFFSHORE SYSTEMS LTD.

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Un sommaire en français de ce rapport est inclus avant la Table des matières.

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16. Abstract

Offshore Systems Ltd. developed its Shipboard Integrated Navigation And Display System (SINADS) with the objective of creating a flexible and reliable integrated navigation-and-display system that included radar overlay. The scope of this development ranged from high resolution charts, integrated ship positioning, radar image overlay, to ARPA (Automatic Radar Plotting Aid) and passage planning capabilities. A six-step design approach was followed: (1) work plan, (2) initial conceptual design, (3) hardware and software design, (4) prototype assembly and coding, (5) system integration and bench testing, (6) and field demonstration and testing.

Hardware design led to the selection of Motorola VME boards, the Radar Scan Converter, and a high-resolution RGB monitor with a custom keyboard. Software design led to the use of UNIX and RTUX as operating systems and C and Assembler for programming languages. The result of the SINADS programme was the successful development of a real-time, modular system prototype, readily expandable into a marketable product that can incorporate ECDIS (Electronic Chart Display and Information System) and ARPA requirements for a truly integrated shipboard navigational system.

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16. Résumé

Offshore Systems Ltd. a conçu son système intégré de navigation et d'affichage de données à bord (SINADS) dans le but de réaliser un système de radionavigation et d'affichage intégré, souple et fiable, intégrant une imagerie radar numérisée. Le système réalisé comporte: des cartes de navigation haute résolution, des systèmes intégrés de radionavigation, des procédés de surimposition d'imagerie radar, une aide de pointage radar automatique et une aide de sélection de l'itinéraire optimal. La démarche d'étude s'est faite en six étapes: i) plan de travail, ii) étude conceptuelle, iii) étude du matériel et des logiciels informatiques, iv) assemblage et codage du prototype, v) intégration des composants et essais au banc, vi) démonstration experimentale et essais en mer.

Le matériel réalisé comporte des cartes VME et des microprocesseurs Motorola, un convertisseur de balayage et un moniteur rouge-vert-bleu comprenant un clavier specialement etudié. Quant au logiciel, il a ete ecrit en langage C et en assembleur et est utilise avec des systemes UNIX et RTUX.

Les essais ont montré que le système SINADS est évolutif et adaptable, qu'il est promis à un intéressant avenir commercial et que l'intégration d'une aide de pointage radar automatique et d'un affichage électronique des cartes de navigation en font un système de radionavigation complètement intégré.

17. Mots clés Navire, marine, base de données hydrographiques, radar anticollision, radionavigation de précision, navigation cartes électroniques de navigation.	18. Diffusion Le Centre de développement des transports dispose d'un nombre limité d'exemplaires.

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The development of the Precise Integrated Navigation System (PINS9000) sponsored in 1984/85 by the Defence Research Establishment Pacific provided OSL with extensive experience and knowledge in the design of integrated navigation or electronic chart systems .

The Shipboard Integrated Navigation (SHINNAV) System Feasibility study [1]* , sponsored in 1986 by the Department of National Defence, widened OSL's expertise in this field and produced preliminary specifications for SINADS.

The Transport Canada Training Institute in Cornwall, Ontario, provided a Sperry MK-16 shipboard radar system, which was used for the in-house testing of the SINADS Radar Scan Converter.

The continuous cooperation with the Canadian Coast Guard - Laurentian Region in 1987 and 1988 provided valuable field experience and user comments relating to the operation of PINS9000. This knowledge was used in the design of SINADS.

The Canadian Marconi Company provided an LN/66 Shipboard Radar System, which was used for SINADS testing and demonstration onboard the M.V. OFFSHORE SURVEYOR.

Canadian Coast Guard also provided the CCGS NICOLET as a test platform for SINADS at-sea evaluations. The CCG Falcon 484 microwave positioning system, and other ship's resources and technical support were used during these trials.

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[*] Numbers in brackets designate references listed at the end of the report.

OSL thanks the crew of the CCGS NICOLET and the supporting technical personnel for their involvement and efforts during the SINADS evaluation.

PREFACE

With the increasing quantity and complexity of navigational information available from various sensors, there is a requirement for the integration and common display of this data on a single bridge display console. In response to this need, Offshore Systems Limited submitted an unsolicited proposal to conceptualize, develop, and evaluate a Shipboard Integrated Navigation and Display System (SINADS).

The objective of this project was to develop and evaluate a hardware and software system that would integrate various ship's navigational sensors including marine radar, provide collision avoidance capability and superimpose this data on a bridge-mounted multiple colour electronic chart. Additionally, a time-selectable real-time record and track history of the ship movements is required to provide an accurate record for future analysis and investigation.

The selective use of ship positioning data, electronic chart data and radar image overlay on a common integrated bridge display should significantly assist the mariner with the real-time navigation of his ship in confined waters. A totally integrated display which includes charts, radar and positioning data does not currently exist.

Offshore Systems Ltd. has been involved in the electronic chart design since the late 1970s, when the first monochrome version of the electronic chart was developed for Dome Petroleum operations in the Beaufort Sea. Since that time, OSL's electronic chart has evolved through several iterations resulting in increased capabilities and applications. In 1985, a Precise Integrated Navigation System (PINS9000) with colour graphics was developed for mine countermeasures research for the Defence Research Establishment Pacific. PINS 9000 has been expanded through many iterations to provide real-time surface ship positioning, sub-surface vehicle positioning as well as harbour management services. In 1985/86, OSL produced a Department of National Defence sponsored SHINNAV (Shipboard Integrated Navigation) System Feasibility Study [1]. This study dealt with the future introduction of the electronic charts in Canadian Naval vessels and produced a number of recommendations including a SHINNAV System

Specification. This system specifications was used as a starting point for the development of SINADS.

SUMMARY

In 1985, Offshore System Ltd. (OSL) submitted to the Science Centre of Supply and Services Canada an Unsolicited Proposal to develop and evaluate a Shipboard Integrated Navigation System (SINADS) for marine navigation and ship collision avoidance.

In response to a recognized need in the marine industry for a standard integrated bridge display console, OSL proposed to investigate a method of integrating all ship's navigational sensors onto one bridge display. This objective was to be achieved by the addition of digital radar image overlay to OSL's existing Precise Integrated Navigation System (PINS 9000).

The project was sponsored by the Transportation Development Centre of Transport Canada, the Canadian Coast Guard, the Department of National Defence, Supply And Services Canada, and the Ministry of Energy, Mines and Resources Canada.

The objective of the project was to conceptualize, develop, demonstrate and evaluate a cost-effective, high speed, high resolution colour graphic shipboard integrated navigation , collision avoidance and display system. The development was based on OSL's experience with PINS9000, and on the results of the SHINNAV (Shipboard Integrated Navigation) System feasibility study [1]. Automatic Radar Plotting Aid (ARPA) and Electronic Chart Display and Information System (ECDIS) requirements were taken into consideration in the system design specifications. The project included a detailed work plan , an initial conceptual design and test procedure, a detailed hardware and software design, a prototype assembly and coding, system integration and testing, field demonstration and testing onboard the M.V. OFFSHORE SURVEYOR in Vancouver, and sea trials and evaluation onboard the CCGS NICOLET in the St. Lawrence River.

After two years of work and approximately eight man-years of engineering effort, a prototype SINADS was developed, constructed and successfully demonstrated. The hardware consists of VME-boards with Motorola 68000 family microprocessors, a custom-designed Radar Scan Converter (RSC), and a high resolution RGB monitor with a custom keyboard. The SINADS software was written

in C and Assembler programming languages and UNIX and RTUX were used as operating systems.

The SINADS prototype includes the following features: high resolution colour charts, integrated ship positioning, radar image overlay, ARPA and passage-planning capabilities, and a user-friendly interface. Some of these functions are at an early stage of development and will require additional work.

During the at-sea evaluations, SINADS proved to be a well designed and flexible system with considerable potential. Although the prototype did not have all its functions fully operational, it was recognized that SINADS can readily be expanded and customized to any specific application. The test results, including comments from the users, were documented and analyzed. Most of the comments referred to minor cosmetic details and the slow performance of the system. Structurally SINADS proved to be sound and reliable. The user interface and friendliness of SINADS has been carefully designed to handle the large SINADS menu tree and the numerous system functions.

In conclusion, OSL has proven the SINADS concept with all the navigation functions integrated in a real-time system. A solid design base was created to ensure that SINADS is modular, expandable, and can be further developed into a successful and marketable product. This product should be able to set a new world standard by incorporating the ARPA and ECDIS requirements into a truly integrated shipboard navigation system.

SOMMAIRE

En 1985, Offshore Systems Ltd. (OSL) a soumis au Centre scientifique d'Approvisionnements et Services Canada une proposition spontanée concernant le développement et l'évaluation d'un système intégré de navigation et d'affichage de données à bord (SINADS), comportant des radars de navigation et anticollision. En vue de doter la marine commerciale d'une console intégrée standard de passerelle de navigation, la proposition d'OSL visait à étudier, en profondeur, une méthode permettant d'intégrer tous les signaux de navigation reçus à bord d'un navire et de les afficher sur une console de passerelle. À cette fin, il s'agissait de surimposer une imagerie radar numérisée sur l'information produite par le système de radionavigation de précision PINS 9000 réalisé par cette même firme. Les coparrains de ce projet ont été: le Centre de développement des transports, Transports Canada, la Garde côtière canadienne, la Défense nationale, Approvisionnements et Services Canada, ainsi que Énergie, Mines et Ressources Canada.

La proposition avait pour but la conceptualisation, la réalisation, la démonstration et l'évaluation d'un système intégré de navigation comportant des fonctions anticollision et d'affichage couleur, haute résolution, rapide et économique. OSL entendait ainsi mettre à profit l'expérience acquise avec le PINS 9000, et conjuguée aux résultats de l'étude de faisabilité sur un système intégré de navigation de bord SHINNAV. Dans leur spécification d'un système proposé, les chercheurs ont pris en considération la nécessité d'intégrer une aide du pointage radar automatique et le système d'affichage électronique de cartes de navigation. La démarche d'étude a comporté les étapes suivantes: élaboration d'un plan de travail détaillé, étude conceptuelle et élaboration d'une procédure d'essai provisoire, étude détaillée du matériel et des logiciels informatiques, assemblage et codage du prototype, intégration et essai du système, démonstration expérimentale à bord du N.M. OFFSHORE SURVEYOR à Vancouver, essais en

mer et évaluation à bord du brise-glace NICOLET de la Garde côtière canadienne dans le Saint-Laurent.

Il a fallu deux années d'études et quelque huit années-personnes de développement technique pour réaliser et mettre à l'épreuve un prototype du système SINADS. Le matériel réalisé comporte des cartes VME et des microprocesseurs Motorola 68000, un convertisseur de balayage spécialement étudié et un moniteur rouge-vert-bleu comprennant un clavier approprié. Quant au logiciel, il a été écrit en langage C et assembleur et est utilisé avec des systèmes d'exploitation UNIX et RTUX.

Le prototype réalisé comporte: des cartes de navigation couleur haute résolution, des systèmes intégrés de radionavigation, des procédés de surimposition d'imagerie radar, une aide de pointage radar automatique, une aide de sélection de l'itinéraire optimal et une interface conviviale. Certaines de ces fonctions, encore au début de leur développement, nécessiteront une recherche plus approfondie.

Les essais en mer ont montré que le système SINADS donne de bons résultats, qu'il est souple d'emploi et qu'il est appelé à un grand développement. Et bien que certaines des fonctions du prototype ne soient pas encore tout à fait au point, le système s'est révélé très évolutif et très adaptable. Les résultats des essais et des interviews auprès des utilisateurs ont été consignés et analysés. Ils ont montré que, à part quelques défauts superficiels et la lenteur du système, celui-ci présente une architecture bien conçue et fiable. Par ailleurs, l'interface homme-machine se caractérise par une convivialité qui facilite l'exploitation du système malgré le très vaste menu d'exploitation et les nombreuses fonctions correspondantes.

En résumé, OSL a montré que SINADS, avec toutes ses fonctions intégrées de navigation, est un très bon système fonctionnant en temps réel, d'autant plus que sa conception modulaire et évolutive en font un produit appelé à un intéressant avenir commercial. De plus, étant le premier à incorporer l'aide de pointage radar automatique et l'affichage électronique des cartes de navigation, il constitue le premier système de radionavigation complètement intégré au monde.

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GLOSSARY OF ABBREVIATIONS AND ACRONYMS

ADM	Advanced Development Model
ARPA	Automatic Radar Plotting Aid
CAS	Collision Avoidance System
CS	SINADS Chart Subsystem
DCS	SINADS Data Communication Subsystem
DND	Department of National Defence
DRAM	Dual-ported RAM
DSS	Department of Supply and Services
ECDIS	Electronic Chart Display and Information System
GDS	SINADS Graphics Display Subsystem
GIS	Graphical Information System
IDC	Interactive Display Console
MSS	SINADS Mass Storage Subsystem
OSL	Offshore Systems Ltd.
PINS 9000	Precise Integrated Navigation System Model 9000
RAM	Random Access Memory
RIS	SINADS Radar Interface Subsystem
ROM	Read Only Memory
RSC	SINADS Radar Scan Converter
RTUX	Real Time UNIX kernel
SAR	Search And Rescue
SHINNAV System	Shipboard Integrated Navigation System
SINADS	Shipboard Integrated Navigation And Display System
STANS	Sonar Tracking And Navigation System
TDC	Transportation Development Centre
TIN	Triangular Irregular Network
UNIX	AT&T multitasking operating system
VME	Versa Module Eurobus
VME bus	micro-computer bus system based on the MC68000
VRAM	Video RAM
VSBbus	local data bus in the VMEbus system
VTS	Vessel Traffic System

1. INTRODUCTION

As a result of an unsolicited proposal submitted to DSS on 17 May, 1985, Offshore Systems Ltd. (OSL) was awarded the Shipboard Integrated Navigation And Display System (SINADS) contract in November 1986. The project was sponsored by the Transportation Development Centre of Transport Canada, the Canadian Coast Guard, the Department of National Defence, Supply And Services Canada, and the Ministry of Energy, Mines and Resources Canada. After two years of development, the prototype SINADS was successfully demonstrated to the Technical Review Committee on 14 November 1988.

1.1. Purpose

The purpose of this development was to create a prototype system, for application as a general purpose navigation display system onboard marine vessels. The automatic one second updates in vessel positioning with radar image overlay as a means of position verification all superimposed on an electronic chart should significantly reduce the incidents of ship groundings and greatly assist in the manual chart plotting routine which is currently required by law. The direct comparison of the radar image to chart outlines will verify the vessel position and reduce the ambiguity in identifying radar targets and land images. The additional functions of target tracking and collision avoidance are major enhancements to a complete integrated navigation system. With real-time recording capability, SINADS can provide a black-box function for accident/incident investigation and law enforcement applications. In general, SINADS could have a significant impact on the future safety of marine navigation by providing a unique integrated navigation and graphics display system that can address all the ships navigational and collision avoidance requirements.

1.2. Objectives

OSL defined the following main objective and seven detailed objectives of the project:

1.2.1. Main Objective

Conceptualize, develop, evaluate, and demonstrate a cost-effective, high speed, high resolution colour graphic shipboard integrated navigation and collision avoidance display system.

1.2.2. Detailed Objectives

The detailed objectives are:

a) Transport PINS functions to VME hardware;
b) Overlay radar image on the electronic chart;
c) Add basic collision avoidance capabilities;
d) Address ECDIS requirements;
e) Prototype user interface;
f) Prototype system concept development;
g) Prototype hardware configuration.

The detailed objectives are further discussed in Appendix A.

1.3. Scope of Development

The scope of development of the SINADS project included the following:

- a) study of operational requirements.
- b) study of environmental requirements;
- c) study of ECDIS requirements;
- d) study of ARPA requirements;
- e) implementation of VME-based hardware development environment;
- f) implementation of UNIX-based software development environment;
- g) implementation of real-time operating system kernel: RTUX;
- h) implementation of TIN (Triangular Irregular Network) chart database;
- i) implementation of Kalman positioning filter;
- j) design and implementation of positioning simulators;
- k) design and implementation of device drivers;
- l) design and integration of the Radar Scan Converter;
- m) design and implementation of improved user interface; and,
- n) study of radar image and chart matching techniques.

2. ASSUMPTIONS AND LIMITATIONS

The SINADS design was based on OSL's experience with PINS, STANS and SHINNAV System developments. The following assumptions and limitations were imposed on the system design:

a) use of a high-resolution 19" RGB monitor for display;
b) use the VMEbus and VSBbus architecture;
c) use of the off-the-shelf VME boards;
d) use of the off-the-shelf graphics board;
e) use of the off-the-shelf mass storage system;
f) modification of the PINS user controls;
g) standard packaging of the prototype;
h) use of UNIX System V development environment;
i) use of RTUX real-time kernel;
j) use of C and Assembler programming languages;
k) development and integration cycle of the Radar Scan Converter;
l) modification and implementation of PINS chart database;
m) display colours dictated by ergonomics and not by paper chart standards;
n) positioning inputs from Falcon 484 microwave positioning system and Sperry MK37 ship's gyro;
o) interface to MK16 and MK127 marine radars;
p) testing onboard the MV OFFSHORE SURVEYOR and CCGS NICOLET.

These assumptions and limitations are further discussed in Appendix B.

3. METHODS USED

The SINADS development was based on OSL's experience with PINS and STANS, and on the results of the SHINNAV System feasibility study [1]. The requirements of ARPA and ECDIS specifications were also taken under consideration. The work was performed in the following stages:

a) detailed work plan;
b) initial conceptual design and test procedures;
c) detailed hardware and software design;
d) prototype assembly and coding;
e) system integration and testing;
f) field demonstration and testing onboard the M.V. OFFSHORE SURVEYOR in the Vancouver harbour; and,
g) at-sea trials and evaluation onboard the CCGS NICOLET in St. Lawrence River.

The SINADS design was performed using the following standard systems analysis technique:

a) definition of system purpose;
b) definition of system outputs;
c) definition and analysis of system inputs;
d) definition and analysis of information processing requirements;
e) definition of system limitations;
f) definition of development objectives;
g) preparation of a conceptual design;
h) preparation of a detailed design;
i) design implementation (prototype assembly);
j) design testing and evaluation (prototype trials);
k) analysis of results;
l) conclusions and recommendations.

4. RESULTS AND FINDINGS OF SINADS DEVELOPMENT

After 2 years of development, a prototype SINADS was successfully tested and demonstrated. The unique features of this prototype SINADS are:

a) VME hardware;
b) C-language software;
c) Multiple colour electronic charts;
d) Precise vessel positioning;
e) User-friendly interactive display console (IDC); and
f) Radar overlay integration.

The above features are further addressed in the following paragraphs.

4.1. VME Hardware

The prototype SINADS computing system was built by customizing the standard MOTOROLA MVME1131 UNIX development system. The chassis of the MVME1131 system was reconfigured to accommodate additional bus backplanes, VME boards, and the Radar Scan Converter (RSC). With the exception of the RSC, available off-the-shelf VME hardware was used. Consequently, the available 1986 VME processing, communications and graphics boards were ordered. Motorola has since discontinued production of some of the selected VME boards and replaced them with higher speed and more capable printed circuit boards. A block diagram of the SINADS computing system, a description of SINADS hardware, and the detailed specifications of the VME hardware are included in Appendix C.

4.2. C - language software

Although based on the original HP-Pascal PINS software, the SINADS "C" software was totally redesigned and restructured to simplify changes and future

software/hardware upgrades. The SINADS program is divided into a number of tasks. The data transfer between tasks is organized via input and output queues, which are lists of memory addresses. The SINADS software structure can readily address all the special PINS and radar overlay features.
A detailed description of the SINADS software is included in Appendix D.

4.3. Multiple Colour Electronic Charts

The SINADS electronic charts are an enhanced version of PINS charts. Triangular Irregular Network (TIN) data structure was implemented to simplify the chart data and facilitate easy chart manipulations, colour fills and feature locations. Although SINADS charts are currently not organized as a world database in latitude and longitude co-ordinates, this capability can easily be added in the future. SINADS charts are currently organized and stored in memory in UTM co-ordinates by hydrographic chart number and can readily be selected from the user interactive keyboard.
A detailed description of SINADS charts is included in Appendix E.

4.4. Precise Vessel Positioning

Like PINS, vessel positioning in SINADS can be addressed by serial interface with the various radio positioning systems. To date, only microwave (Falcon 484, and Miniranger III) positioning systems and ship's gyro have been interfaced with SINADS. The SINADS project developed a successful six-state Kalman-filter algorithm for vessel positioning which utilizes raw input data to calculate an integrated position.
A detailed description of SINADS vessel positioning is included in Appendix G.

4.5. User-Friendly Interactive Display Console (IDC)

The prototype SINADS Interactive Display Console (IDC) consists of a high resolution 1024 pixels x 768 lines RGB monitor, custom membrane keyboard and a keyboard controller (see Figure 1 in appendix C).

The SINADS hardkey/softkey combination addresses the increased menu-tree-structure in SINADS by utilizing 16 hardkeys. Each of these hardkeys has a smaller menu-tree associated with it. Using this approach, the operator at all times knows what menu is in use and can easily switch from one menu to another. The CCG evaluation recognized the advantages of the smaller menu tree structure and emphasized the user-friendliness of this approach.

Detailed description of SINADS user-interface and a draft of the SINADS user's manual are included in Appendix F.

4.6. Radar Overlay Integration

The Radar Scan Converter (RSC) was the most significant new feature not available in PINS, that was integrated into the SINADS system. This feature also represented the greatest technical risk. Regrettably, there was an eight months delay in this subcontract which resulted in the RSC boards being received by OSL just two months prior to the CCG evaluation in October/November 88. This delay resulted in insufficient time to fully implement and test the ARPA and CAS software as the RSC was required for this development. OSL implemented a simple multiple radar target tracking algorithm by using 8-bit radar image data from the RSC's Radar Analysis Buffer upon manual target acquisition. The radar image overlay and target tracking were successfully demonstrated to the technical review committee. Although additional work is required, the concept of radar image to chart matching as a positioning aid was also successfully demonstrated.

A detailed description of SINADS Radar Scan Converter can be found in the Radar Scan Converter Manual included in Appendix H.

5. RESULTS AND FINDINGS OF SINADS EVALUATION

The prototype SINADS was evaluated between October 01st and November 15th 1988, onboard the CCGS NICOLET in the St. Lawrence River between Montreal and Quebec City.

Reports and pictures from the CCG evaluation are included in Appendix I.

6. CONCLUSIONS AND RECOMMENDATIONS

As a result of the SINADS evaluations, a number of recommendations were made relating to the system operation, user-interface, hardware design, and system packaging. In addition, some software and hardware problems were discovered by OSL during this period. The prototype SINADS operated satisfactorily throughout the trials period, however, at this stage, SINADS cannot be considered an operational system.

The SINADS concept has been proven and the major development objectives have been met. These objectives included: transporting PINS9000 functions to VME-hardware and "C" high level programming language, adding radar overlay, providing a higher resolution graphics display, improving the user-interface, and addressing ECDIS, ARPA, and future SINADS expansion requirements. The only item which was not fully demonstrated due to time constraints, was the actual target tracking software. The software for this portion of the development has been written and tested using the OSL simulator. The actual integration and field testing of this software will take place in the near future.

The SINADS development is at a stage where OSL can now clearly define the future system configuration and functionality. To advance SINADS from the prototype stage to the advanced development model stage, the lessons learned during the prototype development phase should be implemented and thoroughly tested in an advanced development model. To achieve this, OSL proposes two parallel development phases. The first phase should concentrate on the enhancement of the SINADS software to address all the desired PINS features utilizing the latest available VME hardware and the medium resolution IMAGRAPH graphics board. In parallel, OSL recommends that the development of a specialized graphics board for high resolution 1280 pixels x 1024 lines graphics display be investigated.

6.1. Recommended Changes to the SINADS Prototype

OSL compiled a list of recommended improvements to the SINADS prototype and then prioritized these improvements according to their operational requirements.

The recommended improvements are grouped as follows:

a) system speed upgrades;
b) user-interface enhancements;
c) ship positioning additions;
d) Radar Scan Converter software enhancements;
e) system environmental packaging upgrade; and
f) system documentation updating.

Each of these improvements is discussed in more detail in the following paragraphs.

6.1.1. System Speed Upgrades

Several comments and recommendations collected during the sea-trials related to the slow system response time. The principal system shortcomings are directly related to the speed limitations of the hardware and the operating system architecture. OSL has clearly recognized that the combinations of the high display resolution, radar image overlay, multiple sensors interfaces, and the complex processing of this data requires much faster VME hardware than that acquired for the prototype. Since the commencement of the SINADS project, the available VME processor speed has increased dramatically. The original SINADS VME CPU boards have been replaced by much faster and more powerful boards. Similarly, significant progress has been made with real-time UNIX-based operating systems. OSL believes that both these technology advancements will correct the SINADS speed limitations. The task of upgrading to faster hardware and a real-time operating system is not difficult owing to the upward-compatibility of the MOTOROLA 68000 family of microprocessors. It is anticipated that these upgrades will significantly improve the system speed, and the response time.

6.1.1.1. SINADS Prototype "Bottle-Necks"

OSL has analyzed the data flow in the SINADS prototype and identified the bottle-necks which waste processing time. The following bottle-necks have been identified:

a) radar image transfer from the Radar Scan Converter to the graphics board;
b) electronic chart data processing, rotation and zoom by the main processor; and
c) multitasking and multiprocessing.

6.1.1.1.1. Radar Image Transfer

The transfer of the radar image from the RSC Radar Image Buffer (RIB) to the graphics board is managed by the SINADS Radar Processor. The RIB data is transferred via the VSBbus to the processor and then retransmitted via the VMEbus into the graphics board VRAM. This process is necessary since the VME graphics board does not have a VSBbus interface. Regrettably, this bus changing process consumes considerable processor time and in addition, it interrupts the other communications on the VMEbus. The result is that chart data cannot be written to the graphics board while radar data is being transferred on the VMEbus. This prototype limitation causes synchronizing and radar/chart alignment problems and slows down the whole system operation. Although the display is updated approximately every two seconds, as the ship's speed increases the misalignment between the radar and the chart increases. The obvious solution to this problem is to provide faster CPU single board computers and acquire or develop a graphics board which has a more powerful graphics engine and both a VMEbus and a VSBbus interface.

6.1.1.1.2. Electronic Chart Data Processing

The electronic chart data processing is performed in SINADS by the main processor. This processor reads the chart data in real-world coordinates from the mass-storage system, builds the colour filled chart in device coordinates and loads it into the graphics board VRAM. This process has to be repeated for every chart change, zoom, rotation, or scroll. This takes approximately 20 seconds to complete in the existing SINADS prototype. The graphics board VRAM is double-buffered so the chart transfer is always performed off screen however, the graphics display is frozen for that 20 seconds period. This delay is clearly undesirable. To overcome this major problem, the best solution is a purpose-built graphics board equipped with a fast Graphics System Processor. This graphics board should be able to receive a display list containing chart data in real-world coordinates. The graphics processor could then manipulate this data to create the required chart zoom, and rotation. With the exception of the initial chart data transfer, this would significantly reduce the processing load on the main processor and dramatically speed-up the entire system. In the case of multiple-console system design, a dedicated graphics boards is the only viable solution.

Until a dedicated graphics board is developed, the optimization and development of an advanced SINADS system should concentrate on a medium resolution (640 pixels x 480 lines) display. OSL believes that faster chart manipulations are more important than higher resolution in the near term. However, the system design should ensure that the upgrade to a high resolution (1280 pixels x 1024 lines) display can be easily accomplished at a later date.

6.1.1.1.3. Multitasking And Multiprocessing

SINADS uses a combination of UNIX and RTUX operating systems with OSL multitasking extensions. At the time SINADS was conceptualized, there was no real-time UNIX-based operating system available, which could meet both the development and the real-time application requirements. UNIX is not a real-time operating system, and RTUX does not provide the file utilities required by SINADS. The present mixture of operating systems in SINADS is not optimized for speed and has several obvious inefficiencies. One of the recently developed UNIX-based real-time operating systems combined with the proposed higher speed hardware should address the system speed and flexibility requirements. OSL considers an Advanced Development Model (ADM) SINADS as an essential requirement to building a successful operational SINADS.

6.1.1.2. System Speed Upgrade Recommendation

OSL proposes that the main objective of the Advanced Development Model SINADS should be system speed through the following improvements:

a) use of the new-generation VME hardware;
b) implementation of a real-time UNIX-based operating system;
c) optimization of SINADS software for increased speed;
d) use of medium resolution (640 pixels x 480 lines) graphics; and
e) development of a specialized VME graphics board.

6.1.2. User Interface Enhancements

Numerous comments and suggestions received during the at-sea evaluations were related to the user-interface portion of the system. Direct user-interface comparisons with PINS9000 were provided by TDC and by the CCGS NICOLET crew. The results of this evaluation are summarized in the following paragraphs.

6.1.2.1. System Screens

PINS screens have fixed graphic windows and fixed alphanumerics. This means that within any screen configuration the size of the chart window(s), as well as the location, size, and content of the alphanumerics cannot be changed in real-time. PINS features a variety of off-line editors and system configuration tools which provide for the customization of PINS screens. A number of screen layouts can be preconfigured and stored in the system memory. In order to change the contents of the screen alphanumerics, the operator must switch to a different screen configuration. Experience with operational PINS systems indicate that the screen editors are rarely used by the ship operators. During the initial installation a few screen layouts are configured by the OSL technician to address the customer requirements and they are rarely modified afterwards.

SINADS screen configurations have fixed graphic windows and selectable alphanumerics. The screen configuration is divided into the chart window and a number of alpha-boxes. The operator can select the data and the size of the alphanumeric data to be displayed in each box. This approach allows the operator to select and display the highest priority data of interest . Various screen layouts can be achieved through the use of ASCII configuration files. These files are created by OSL and supplied with the system, and describe the size and the location of the graphics windows and the location of the alpha-boxes. Currently, the SINADS prototype only provides a single chart window however, the software is designed for multiple windows. There is however one restriction and that is the radar image can only be provided as an overlay on one of the display windows at a time.

Initial feedback from the at-sea evaluations indicate that the SINADS screen configurations with variable alpha-boxes, provided the operator with the system flexibility that was required. This configuration is also convenient during the testing and debugging phase when frequent changes of screen layouts are common. The concept of flexible alpha-boxes allows the operator to display only the required data which is considered essential at the time. Several observers also recommended that the size of the graphics area should be maximized.

OSL believes that screen layouts and configurations play an important role in the overall system operation. System performance is often judged by the quality of the display. Optimization of screen configurations is an essential component of the ADM SINADS.

6.1.2.2. User-Functions

The prototype SINADS does not provide all the user-functions available in PINS. Additionally, some of the existing SINADS functions (such as; line and station editor, record and playback function) will also require refinement and debugging in order to bring them to full operational status. The modular design of SINADS software and the menu structure ensures that all user functions can be readily added. Ultimately, SINADS will be able to provide all the unique features of PINS as well as many radar features. Radar target tracking, collision avoidance, and continuous chart capability are a few examples of these extra features. Additional user functions will gradually be implemented in SINADS in accordance with their market priority.

6.1.2.3. User-Interface Design

There were four principal criticisms of the SINADS user-interface. First and foremost the display cursor was too slow and inaccurate. Secondly, the monitor had insufficient brightness control for the bridge ambient light conditions. Thirdly, the display colour combinations were not optimized. And finally, it was noted that the membrane keyboard required some form of tactile feedback and background lighting. Alternate input devices such as a trackball or a touchpad, were suggested as replacement for the membrane keyboard.

Most observers of the SINADS at-sea evaluations acknowledged that the design of the user-interface was very user-friendly. OSL analyzed the PINS functions and the planned radar functions and assigned each functional group a dedicated hardkey. This technique allows a large menu tree to be subdivided into sixteen smaller trees which results in the simplification of the user interface and faster access to the bottom-menu-level functions.

Although the 16 functional group hardkeys adequately address the large menu requirements, numerous improvements in the individual menu trees can still be achieved. Improvements in the radar controls are an essential requirement.

6.1.2.4. User-Interface Design Recommendations

OSL recommends the enhancement of the SINADS user-interface by:

a) further simplification and debugging of the user-interface design;
b) incorporation of new user-controls (trackball, touchpad, etc);
c) redesign of SINADS screens in order to maximize the graphics area;
d) addition of new user-functions and graphics tools; and
e) improvement of display clarity and legibility in high ambient light conditions.

6.1.3. Ship Positioning Additions

The SINADS prototype was tested with navigation inputs from a microwave system and a ships gyro. The positional accuracy of SINADS and its Kalman filter was found to be essentially equivalent to the Falcon 484 console during the CCG NICOLET evaluations.

Since most ships are fitted with LORAN C radio positioning receivers, it is recommended that SINADS be interfaced to a LORAN C receiver. The SINADS Kalman filter was designed for additional navaids inputs. By utilizing an approximate vessel position from a radio navaid and the radar image to chart matching technique, a powerful real-time inshore positioning capability can be provided by SINADS when interfaced to existing ship fitted radars and LORAN C. The implementation of this unique blind pilotage capability is an important feature that needs to be further addressed in the SINADS ADM.
A number of additional user-functions such as crosstrack, CTS (course-to-steer) and ETA (estimated-time-of-arrival) and error ellipse should also be added. The related radar data such as anti-collision capabilities and target tracking should similarly be addressed.

6.1.3.1. Ship Positioning Additions Recommendation

To enhance the SINADS positioning capabilities OSL recommends the addition of the LORAN C interface and the development of new positioning-related user-functions.

6.1.4. Radar Scan Converter Software Enhancements

A significant part of the SINADS prototype development was dedicated to the integration of the radar image overlay on the electronic chart. A SINADS Radar Scan Converter (RSC) that can interface with any quality marine radar was developed and tested. The radar video, trigger and antenna synchro data are digitized then scan converted to produce a 1024 pixels x 1024 lines raster radar image. A number of radar signal processing functions were also incorporated into the RSC, including digital gain and STC control, FTC, as well as buffer, radial and azimuth averaging functions. Due to the complexity of these operations only a limited number of combinations of these functions were tested. During the CCG NICOLET sea-trials, some problems with the radar antenna synchro to digital conversion were encountered. The image distortion at the extremities was quickly corrected once the problem was analyzed. The radar target tracking software was not fully implemented and tested due to the unexpected delays and complications in the RSC CAD-layout and board fabrication. The RSC user-interface controls which were hastily implemented were also found to be inadequate. A major effort is required to enhance all aspects of the RSC image processing and user-interface control software. Although the RSC has considerable image processing capabilities, OSL recommends delaying this area of development until SINADS becomes an operational system.

6.1.5. System Environmental Packaging Upgrades

The SINADS prototype construction was based on an off-the-shelf Motorola VME development system. This system was not ruggedized or environmentally protected to meet sustained shipboard operational requirements. Similarly, the user console was built using a standard 19" RGB Monitor and a prototype membrane keyboard. The task of upgrading the SINADS hardware to meet the environmental requirements is not difficult. The VME hardware including the RSC, is by design rugged and shock resistant. The move to newer, faster, and more capable VME boards will significantly reduce the total number of boards and should result in a smaller more reliable computer package.

The most fragile component in the prototype system is the hard disk drive . The hard disk drive is currently used to store system software, configuration files, chart data, and recorded vessel positioning information. During the development and testing phases, software changes are necessary consequently, hard disk drives are desirable. However, upon completion of the development cycle, proven system software can be permanently stored in onboard EPROM. Similarly, variable configuration files can be moved to non-volatile battery-backed RAM. Floppy disks or optical storage can then be used for the chart data, and vessel positioning recording. By utilizing these alternate memory storage components the fragile hard disk can be eliminated.

The RGB monitor is the most difficult item to handle from a packaging perspective. The size, weight, power and cooling requirements result in a bulky package which is not ideal for shipboard operations. The low brightness of the CRT combined with the ambient light reflections, make the the task of installing the monitor on the bridge even more difficult. Until more compact colour display technologies are available, the RGB monitor is the only suitable colour display. The SINADS ADM should concentrate on the selection of a better RGB monitor and the integration of this monitor with new user controls into an environmentally protected package. OSL recommends that an ADM SINADS be tested in one of the Canadian Forces environmental testing facilities at some future date.
OSL recommends the development of a new SINADS hardware package through the following tasks:

a) selection and purchase of advanced integrated VME boards;
b) selection and purchase of ruggedized disk drives;
c) gradual transfer of system software to onboard EPROM and non-volatile RAM;
d) design of environmentally protected computer chassis;
e) selection and purchase of a better RGB monitor;
f) selection and purchase of new user-controls; and
g) design of user-console
h) integration of system hardware.

6.1.6. System Documentation Upgrades

OSL recommends the upgrade of the prototype SINADS operations manual to include all the enhancements and additions developed in the next phase of development.

7. REQUIREMENT

The Canadian Coast Guard and the Canadian Navy have requirements for an operational SINADS for the following applications:

a) precise vessel positioning;
b) general inshore navigation;
c) open-ocean navigation;
d) CCG Search and Rescue (SAR) operations;
e) CCG Vessel Traffic Services (VTS) operations;
f) Naval shipboard navigation and tactical displays; and
g) Naval mine countermeasures operations.

Items d through g will require some custom hardware and software to optimize SINADS for these specific applications once SINADS is an operational system. The operational requirements are further discussed in Appendix J.

8. MARKET POTENTIAL

The Canadian Navy's twelve ship Maritime Coastal Defence Vessel (MCDV) program has a definite requirement for three or four SINADS tactical display systems per ship. OSL is well positioned to provide SINADS to the Navy as an order for two systems is anticipated shortly for the Navy's Mine Countermeasures Auxiliary (MCMA) vessels. These vessels are being acquired as interim vessels until the MCDV are built in 1992. The Navy has plans for a total of 47 MCDV's over the next 25 years.

The USCG Headquarters (Ship Systems) has expressed considerable interest in SINADS due to the integrated navigation capability with electronic charts and radar overlay. USCG/HQ have stated that 80 ships will be refitted over the next five years and most of the larger cutters will require integrated navigation systems like SINADS. The CCG and Fisheries Protection Vessels have requirements for integrated navigation systems for Search and Rescue operations as well as surveillance operations of the 200 nautical mile economic protection zone.

The Canadian Coast Guard Vessel Traffic Services (VTS) will be spending $50 M over the next 10 to 15 years for new and upgraded VTS facilities. To the best of OSL's knowledge, SINADS is the only raster scan display with charts and radar overlay capability made in Canada that can address the VTS requirements. Clearly, there is a considerable market potential in Canada and the USA for SINADS. OSL's PINS is considered to be a world leader in integrated navigation systems however, SINADS with radar overlay represents an order of magnitude advance in the state-of-the-art of integrated navigation or electronic chart systems.

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APPENDIX A - DETAILED OBJECTIVES OF SINADS DEVELOPMENT

The detailed objectives of SINADS development are described in the following paragraphs.

a1. PINS functions on VME hardware

The development of PINS9000 was based on the Hewlett Packard 200 and 300 family of computers. These computers were known for their reliability and ruggedness and were used widely for survey and scientific applications. The design of the Hewlett Packard hardware and software however, posed serious restrictions on the system configurability and expandability. The single-microprocessor design of Hewlett Packard equipment is limited for the following reasons:

a) it does not allow the addition of extra processors for increased computing power;
b) the bus-size and chassis-size restrictions limit the amount of RAM and number of devices which could be interfaced with HP computers;
c) the software written in HP-Pascal is not transportable to other computers;
d) the HP graphics board has a very limited growth potential; and
e) the hardware design is proprietary to HP and therefore not available from other suppliers.

The combination of single-source hardware, limited flexibility and high cost has prompted OSL to look for alternate solutions. As a part of the SHINNAV Feasibility Study [1] , OSL investigated various hardware/software solutions suitable for the development of an "ideal" navigation system. The VME hardware based on Motorola 68000 family of microprocessors was selected. Furthermore the study recommended UNIX and it's real-time kernel for an operating system and C and Assembler programming languages. Since the SHINNAV Feasibility Study [1] similar hardware/software combinations have been successfully implemented by DND. The SINADS development has followed the recommendations of the SHINNAV Feasibility Study [1].

a2. Radar Image Overlay

The PINS9000 integrates various ship navigation sensors on a single graphic display with the exception of radar imagery. The interface of this important navigational sensor required specially designed electronics with high speed processors. With the move to VME hardware, it was possible to design a Radar Scan Converter (RSC) which could fit into the same VME chassis and communicate with the main computer over a private bus. The radar overlay superimposed on electronic charts provides two very important features. Firstly, the electronic chart clearly resolves the radar image ambiguity by identifying land clutter from surface contacts. Secondly, by adjusting the radar image to match the electronic chart an effective radar positioning or blind pilotage system can be provided to the mariner. The radar overlay capability was the major innovative development in the SINADS project.

a3. Basic Collision Avoidance Capabilities

Collision Avoidance System (CAS) is an integral feature of modern radars. Consequently, a CAS capability is a desirable feature to be added to SINADS. The Automatic Radar Plotting Aid (ARPA) standards were analyzed and the feasibility of implementing these features into SINADS was assessed and provided for.

a4. ECDIS Requirements

OSL has significantly contributed to the establishment of Electronic Chart Display and Information System (ECDIS) international standards via the Canadian Hydrographic Service. OSL recognizes that at some future date, these electronic chart standards will be implemented. Consequently, SINADS was designed to accommodate these future standards.

a5. Prototype User Interface

The design of the PINS user-interface was based on the directed-syntax softkey menus and a custom keyboard attached to the RGB monitor so that the softkeys are aligned below the menu windows. This concept proved to be simple and effective. The SINADS concept utilizes the directed softkey approach but simplifies the menu tree by subdividing it among 16 functional keys which in turn results in 16 smaller menu trees. This concept was easy to use and proved very effective during the at-sea evaluation.

a6. Prototype System Concept Development

An objective of the SINADS design was to create a modular hardware and software system. This technique should simplify the process of system changing and debugging, and also facilitate future enhancements. Similarly, the use of structured programming techniques and a standard programming language would also facilitate future upgrades to faster hardware.

a7. Prototype Hardware Configuration

The selection and design of the the SINADS prototype hardware should allow for the future upgrade to a production system. The design should address the packaging, interfacing, environmental as well as ergonomic requirements. In addition, the design should address future enhancement of the prototype to a cost-effective, attractive and marketable product.

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APPENDIX B - DEVELOPMENT ASSUMPTIONS AND LIMITATIONS

The assumptions made, and limitations imposed on the design are discussed in the following paragraphs.

b1. 19" RGB Monitor

The display of colour charts, radar imagery and other alphanumeric and graphic information requires a high resolution colour display. The display should allow the selection of at least 32 colours and their shades out of a full colour palette. The resolution should be at least 1024 pixels by 768 lines. This display resolution is dictated mostly by the visual appearance of lines, characters and symbols. In addition, the size of the display is dictated by the quantity of data to be displayed and the current ARPA requirements. These requirements state that the size of the display should be at least 340 mm in diameter.

At the current state of the display technology, only a 19" RGB analog monitor can come close to filling all requirements. The raster mask of the 19" CRT is 360 mm wide and 270 mm high. Larger high-resolution RGB monitors are at present prohibitively expensive.

The selection of a 19" RGB monitor also has its drawbacks. The monitor is heavy, bulky, it consumes considerable power and requires cooling. Environmental protection from shock, vibration and moisture is difficult. Most monitors are susceptible to image distortions caused by the ship turning, and require frequent degaussing. A combination of the low brightness, poor CRT contrast, and outside light reflections makes an RGB monitor less than ideal in high ambient light conditions. All these drawbacks makes the installation of a 19" RGB monitor difficult, particularly on smaller ship bridges.

At the present time however, a 19" RGB monitor is the only solution which can meet SINADS requirements.

b2. VMEbus and VSBbus Architecture

As a part of SHINNAV Feasibility Study [1] , OSL investigated various hardware solutions suitable for the development of a state-of-the-art navigation system. The

VMEbus and VSBbus architecture was recommended as this architecture has been accepted by the DND as the best suited for new developments.

b3. Off-the-shelf VME Boards

The VME hardware based on Motorola 68000 family of microprocessors were selected. It consisted of the state-of-the-art processor boards, dual ported memory boards, disk controller, and a 6-port RS232 communication controller board. Motorola has since introduced more powerful and faster microprocessors and discontinued production of some of the selected VME boards by replacing them with higher speed and more capable integrated boards.

b4. Off-the-shelf Graphics Board

OSL researched the graphics board market and selected the IMAGRAPH Corporation VME graphics board model No. IP 1076-10-A-2.5-N-V. The graphics board was based on a HITACHI HD63484U ACRTC Graphics Processor and a Brooktree Bt458 Colour LUT. The 2.5 Mbyte of onboard 8-bit-deep VRAM allowed the double-buffering of the 1024 pixels x 768 lines screen graphics containing the electronic chart, the alphanumerics, ship's outline and track history, as well as other on-screen graphics tools . The additional 0.25 Mbyte of the 2-bit-deep overlay allowed display of the radar image on the top of this graphics data. The design of the IMAGRAPH graphics board allowed the direct access to the VRAM from the VME bus. The selected graphics board was the only board available on the market which could come close to filling the SINADS requirements. The maximum size of the VRAM did not allow the originally planned implementation of the high resolution 1280 pixels x 1024 lines display in the prototype SINADS.

b5. Mass Storage

The prototype SINADS was based on the Motorola MVME1121 and MVME1131 development systems. Both systems were supplied with a Winchester hard disk and a floppy disk drives. Subsequently, these mass storage media were utilized for the prototype SINADS. Hard disk drives are not the ideal memory system for shipboard applications due to their susceptibility to shock and vibration. At the development stage however, the hard disk offers the flexibility necessary for implementation and testing of the system software.

b6. User Controls

The design of the prototype SINADS user-controls was limited to the modification of the PINS membrane custom keyboard. This successful PINS design provided the mariner with a simple user interface. The SINADS keyboard design added an additional array of 16 function keys, four diagonal cursor keys and a DEGAUSS and POWER keys to a standard PINS keyboard. The electronics necessary to control these extra keyboard functions were also developed as part of the SINADS project.

b7. Packaging

The prototype SINADS used a standard 19" Motorola development system VME chassis and a power supply. This chassis offered good flexibility in the development stage when boards had to be frequently removed and reconfigured. The easy access to bus backplanes facilitated system testing. Regrettably this standard chassis did not offer the necessary environmental protection for the shipboard application. Also the exposed board reset switches and the location of system connectors was not desirable.

b8. UNIX System V Software Development Environment

The UNIX System V supplied with the MOTOROLA development system offered a variety of programming and debugging tools as well as the multi-user, multitasking environment, which was ideal for the development of the C language software. Regrettably the UNIX system was not designed for the real-time operations.

b9. RTUX Real Time Kernel

The development of a navigation system which could handle the electronic charts, ship positioning, user-interface and radar image overlay required a real-time operating system. Regrettably, UNIX System V did not offer such capabilities. Consequently OSL had to find an appropriate real-time, UNIX-compatible operating-system kernel. In 1986 a suitable real-time UNIX based operating system was not available consequently, OSL selected Emerge Systems RTUX and addressed the file utility requirements by combining RTUX with UNIX. This approach was less than ideal but it was the only available option at the time.

b10. C and Assembler Programming Languages

The SHINNAV System Feasibility Study [1] recommended that the standard C programming language be used. The UNIX System V is mostly written in C and provides excellent support for C language development. A standard (Kernighan and Ritchie) version of C was utilized with some of the low level extensions written in Assembler. This approach ensures that SINADS code can be easily transported to any other computer which uses a standard C compiler.

b11. RSC Development and Integration Cycle

The parallel development of the Radar Scan Converter with the rest of the SINADS created some limitations in the design phase. The actual implementation and integration of the radar target tracking software had to be delayed until the RSC was integrated and tested in the system. The tracking software was not fully developed prior to the at-sea evaluation period however, the basic concept was demonstrated.

b12. Chart Database

The SINADS chart database design was structured for future expansion into a continuous world hydrographic database. The contents of the SINADS database was made equivalent to PINS database. The implementation was limited to the size of the single paper chart, and contained land, foreshore, and two depth contours. The navaids were located in a separate file, in order to allow their selective display. This concept was designed to facilitate chart updates and specifically the updates of chart navaids. All data is digitized and stored in the SINADS chart database in UTM coordinates. Due to this fact a central UTM meridian which was used for chart digitizing has to be specified by the user before this chart is selected from the SINADS menu. SINADS can store multiple charts and each charts can be selected on-line as long as the central meridian is the same.

The use of the Triangular Irregular Network will allow for the future expansion of the SINADS chart database to include more features as recommended in the ECDIS specifications.

b13. Display Colours

The proper selection of colours on an RGB monitor is a very important factor in the ergonomic system design. For optimum operator perception, the number of colours should not exceed eight. Each of these colours should be used for different object types. In addition, only four shades of each colour should be used to show the intensities of these objects as the human eye reacts differently to various colour combinations.

In accordance with these contraints OSL limited the number of SINADS display colours to avoid any undesirable visual perception problems.

b14. Navaids

The ship positioning in SINADS was based on the raw range inputs from the Falcon 484 microwave positioning system and on the gyro readings form the ships Sperry MK37 gyro.

b15. Radars Used

SINADS RSC was designed to be interfaced to any quality marine radar. The SINADS prototype was tested with the SPERRY MK16, Marconi LN66, and a SPERRY MK127 marine radars.

b16. Test Platforms

SINADS was tested and evaluated onboard the M.V. OFFSHORE SURVEYOR in the Vancouver Harbour , and the CCGS NICOLET in the St. Lawrence River. The system positioning algorithms was thoroughly tested during severe ship manoeuvring, typical for the survey work performed by the CCGS NICOLET. The SINADS was not tested in various sea-state conditions.

APPENDIX C - SINADS HARDWARE DETAILS

The prototype SINADS block diagram is shown in Figure 1.

c1. SINADS Subsystems

The prototype SINADS computing system consists of the following subsystems:

a) Chart Subsystem (CS);
b) Graphics Display Subsystem (GDS);
c) Data Communications Subsystem (DCS);
d) Mass Storage Subsystem (MSS);
e) Radar Interface Subsystem (RIS); and
f) Radar Scan Converter (RSC).

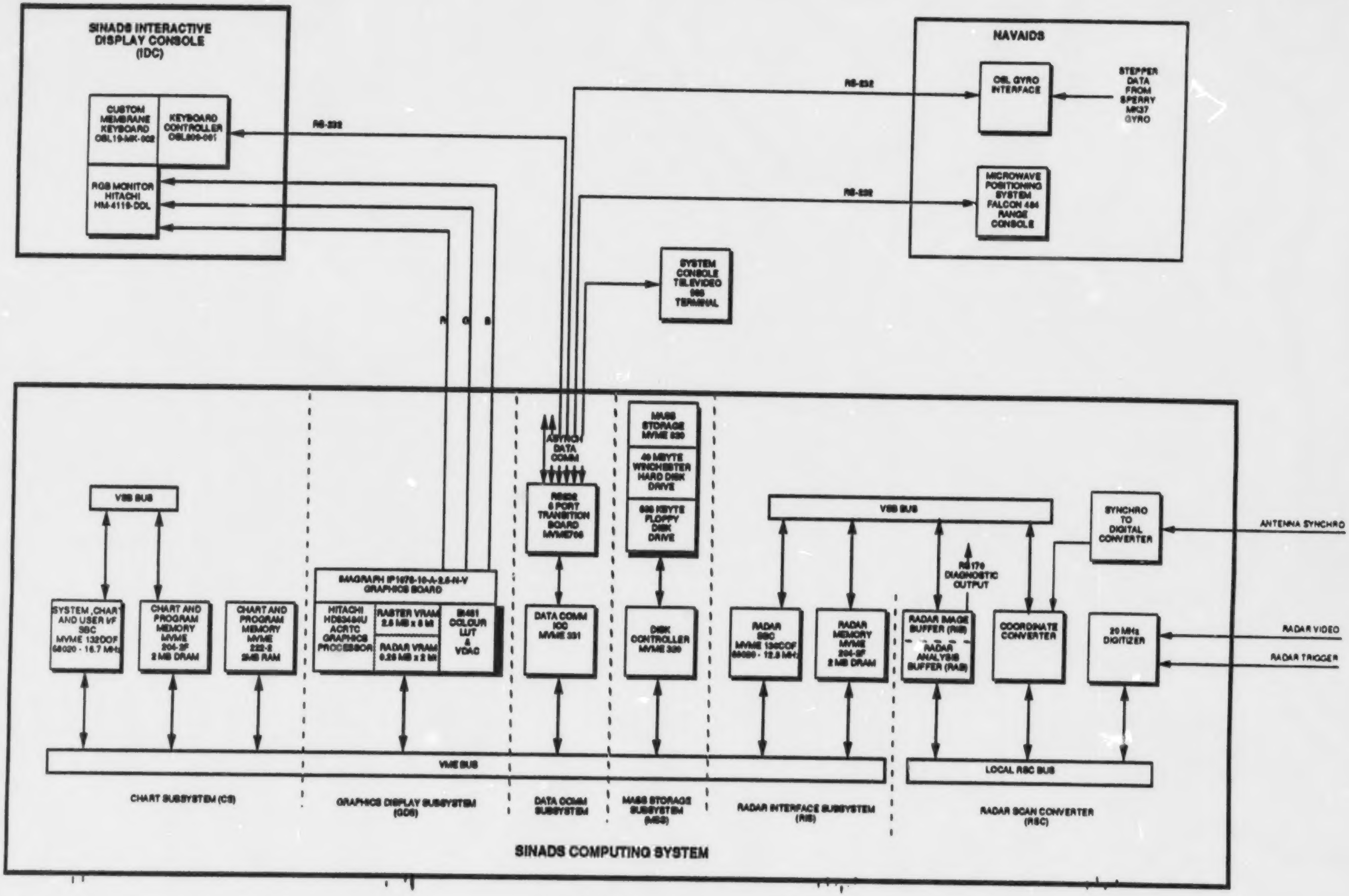
The subsystems are described in the following paragraphs.

c1.1. Chart Subsystem (CS)

The SINADS chart subsystem consists of the following boards:

a) MVME132DOF - single board computer (SBC);
b) MVME204-2F - RAM board with 2 Mbyte of DRAM; and
c) MVME222-2 - RAM board with 2 Mbyte of RAM.

The single board computer performs four functions: it is the main UNIX system controller, it builds electronic charts from data stored on the hard disk and loads them into the graphics board, it runs positioning filters, and it controls the user interface functions. The RAM boards are used for temporary storage of system code and data. The main SBC communicates with the memory boards via the VME bus. In addition, the SBC uses the VSB bus for data


SINADS INTERACTIVE DISPLAY CONSOLE (IDC)
CUSTOM MEMBRANE KEYBOARD OBL19-MK-002
KEYBOARD CONTROLLER OBL800-001
RGB MONITOR HITACHI HM-4119-DOL
RS-232
R
G
B
NAVAIDS
OBL GYRO INTERFACE
STEPPER DATA FROM SPERRY MK37 GYRO
RS-232
MICROWAVE POSITIONING SYSTEM FALCON 484 RANGE CONSOLE
RS-232
SYSTEM CONSOLE TELEVIDEO 955 TERMINAL
VSB BUS
SYSTEM, CHART AND USER I/F SBC MVME 132DOF 68020 - 16.7 MHz
CHART AND PROGRAM MEMORY MVME 204-2F 2 MB DRAM
CHART AND PROGRAM MEMORY MVME 222-2 2MB RAM
IMAGRAPH IP1076-10-A-2.5-N-V GRAPHICS BOARD
HITACHI HD63484U ACRTC GRAPHICS PROCESSOR
RASTER VRAM 2.5 MB x 8 bit
RADAR VRAM 0.25 MB x 2 bit
B461 COLOUR LUT & VDAC
ASYNCH DATA COMM
RS232 6 PORT TRANSITION BOARD MVME706
DATA COMM ICC MVME 331
MASS STORAGE MVME 820
40 MBYTE WINCHESTER HARD DISK DRIVE
655 KBYTE FLOPPY DISK DRIVE
DISK CONTROLLER MVME 320
VSB BUS
RADAR SBC MVME 130COF 68020 - 12.5 MHz
RADAR MEMORY MVME 204-2F 2 MB DRAM
RS170 DIAGNOSTIC OUTPUT
RADAR IMAGE BUFFER (RIB)
RADAR ANALYSIS BUFFER (RAB)
COORDINATE CONVERTER
SYNCHRO TO DIGITAL CONVERTER
ANTENNA SYNCHRO
20 MHz DIGITIZER
RADAR VIDEO
RADAR TRIGGER
VME BUS
LOCAL RSC BUS
CHART SUBSYSTEM (CS)
GRAPHICS DISPLAY SUBSYSTEM (GDS)
DATA COMM SUBSYSTEM
MASS STORAGE SUBSYSTEM (MSS)
RADAR INTERFACE SUBSYSTEM (RIS)
RADAR SCAN CONVERTER (RSC)
SINADS COMPUTING SYSTEM

SINADS
BLOCK
DIAGRAM

Figure 1

transfers to and from the DRAM board. The main SBC communicates with the radar SBC via the VME bus using the Message Clerk software.

c1.2. Graphics Display Subsystems (GDS)

The SINADS Graphics Display Subsystem is based on the IMAGRAPH VME graphics board Model No. IP1076-10-A-2.5-N-V. The graphics board contains a Hitachi HD63484U ACRTC graphics processor, 2.5 Mbyte of 8-bit deep main VRAM, an additional 0.25 Mbyte of 2-bit deep overlay VRAM, a Brooktree Bt458 RAMDAC, and a VMEbus interface. The filled chart data, ship's outline and track, as well as other user interface graphic and alphanumeric data are loaded into the main VRAM by the main processor via the VME bus. The chart images are transferred to the overlay VRAM by the Radar SBC also via the VME bus. The radar image overlayed on the top of the electronic chart is scanned out to the SINADS interactive display console as a non-interlaced, RGB analog signal, with a 60 Hz refresh rate.

c1.3. Data Communications Subsystem (DCS)

The SINADS Data Communication Subsystem consists of an Integrated Communication Controller (ICC) board MVME331, and a serial port transition board MVME705. Combined, these two boards provide six (6) serial RS232C ports used for data communication with sensors, system console and the IDC keyboard. The 68010 processor on the ICC board controls the serial data flow and buffering functions.

c1.4. Mass Storage Subsystem (MSS)

Prototype SINADS uses a 5-1/4" - 40 Mbyte Winchester hard disk drive for mass data storage. It contains the operating system files, the SINADS software, the electronic chart data, system configuration files, the station and lines files, as well as the positioning data recording files. In addition, a 5-1/4" - 655 Kbyte floppy disk drive is used for software and chart updates. The positioning data recording files also can be transferred to a floppy disk if required. A disk controller MVME320 board provides interface of the mass storage to the VME bus.

c1.5. Radar Interface Subsystem (RIS)

The SINADS Radar Interface Subsystem consists of a radar MVME130COF single board computer (SBC), and a radar MVME204-2F DRAM board. The radar SBC controls the Radar Scan Converter (RSC) , performs radar target tracking functions, and transfers the 2-bit-deep radar images from RSC radar image buffer to the graphics board overlay VRAM. The radar SBC communicates with the main-SBC via the VME bus using the Message Clerk software. The radar SBC also communicates with the RSC buffer and converter boards via the VSB bus. The DRAM board is used for temporary storage and execution of the RSC driver and the radar-target-tracking software.

c1.6. Radar Scan Converter (RSC)

The SINADS Radar Scan Converter consists of four printed circuit boards; a Synchro to Digital Converter (S/D Board), a Digitizer Board, a Converter Board, and a Buffer Board. The S/D Board converts the synchro signals from the radar antenna to a digital format and send the digital antenna positions to the Converter Board. The Digitizer Board accepts the radar video and trigger signals and digitizes each radar radial at a maximum rate of 20 MHz and 8-bit resolution. The digitized 8-bit radial data is transferred to the Converter board, where it is translated to cartesian coordinates. The Converter board writes the raster radar data into the Buffer Board's DRAM. The Buffer Board is organized in two sections; a Radar Image Buffer (RIB), and a Radar Analysis Buffer (RAB). The Converter board writes the full eight bits of radar data into the RAB, and only two selected bits into the RIB. The radar-SBC uses the RAB for target tracking, and transfers the RIB data to the graphics board's overlay VRAM. The Digitizer, Converter and Buffer boards communicate via a proprietary RSC-bus. The control of the RSC and the transfer of radar data is performed by the radar-SBC, which communicates with the Converter and Buffer boards via the VSBbus.

c2. Computing System Data Buses

The prototype SINADS computing system consisted of four separate data buses; one main VMEbus, two local VSB-buses, and one local, proprietary RSC-bus. SINADS block diagram in Fig.1 illustrates the bus connection scheme.

c3. VME Hardware Specifications

Copies of the following VME hardware specifications are attached:

a) Motorola MVME 1131 - VMEbus Modular System with SYSTEM V/68 (C-7);
b) Motorola MVME 945-1 - VMEbus Chassis Assembly (C-14);
c) Motorola MVME 130 - VMEmodule 32-bit Monoboard Microcomputer (C-20);
d) Motorola MVME 331 - VMEmodule Intelligent Communication Controller (C-27);
e) Motorola MVME 320 - VMEbus Disc Controller (C-36);
f) Motorola MVME 204 - VMEmodule 2Mb Dynamic RAM (C-40);
g) Motorola MVME 222-2 - VMEmodule 2Mb RAM (C-44);
h) Motorola MVME 820 - Mass Storage (C-47);
i) Motorola MVME 705 - 6-channel Serial Transceiver Module (C-51); and
j) IMAGRAPH Advanced Color Graphic Controllers for VME bus (C-54).

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MOTOROLA
MICROSYSTEMS PRODUCTS
TECHNICAL DATA

by SYS1131UY341 DD

SYS1131UY341

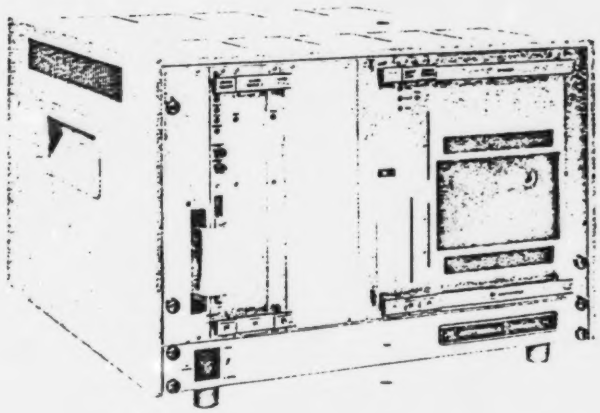
VMEbus Modular System With SYSTEM V/68™

FEATURES:

- SYSTEM V/68, Release 2
- MVME204-2 2Mb Dual-Ported DRAM with MVMX32bus Interface
- MVME320A-1 Disk Controller
- MVME350 Streaming Tape Controller
- MVME331 6-Channel Serial Communications Controller
- 70Mb Winchester Disk Drive
- 655Kb Floppy Disk Drive
- QIC-02 Cartridge Streaming Tape Drive
- Eight RS-232-C Ports (Total)
- MVME131XT Microcomputer with
  - MC68020 Microprocessor (16.67 MHz)
  - MC68881 Floating Point Coprocessor (16.67 MHz)
  - MMB851 Memory Management Unit
  - 16Kb Instruction/Data Cache
  - Two Sockets for JEDEC 28-Pin ROM/EPROM Devices
  - Two Sockets for JEDEC 28-Pin RAM/ROM Devices
  - Two Multi-protocol Serial Ports
  - A32:D32 VMEbus Interface
  - MVMX32bus Interface*
- System Level Diagnostics

MVME945 CHASSIS FEATURES

- 19" Rack Mount Chassis with Tabletop Enclosure
- Transverse 400 W Mid-Chassis Power Supply
- 12-Slot, VMEbus-Compatible Card Cage
  - A32:D32 Backplane
- Accommodates up to 20 Rear-mounted 80 mm I/O Transition Modules



The greatest advantage of a VMEbus-based system is its modularity. To a core system, add only those software and hardware components required for the application. Then serve a new application by changing only a component or two.

The SYS1131UY341 with SYSTEM V/68, is a versatile core system configured using standard VMEbus modules. Supplied in 19" rack-mountable chassis with an enclosure for desktop use, the system has ample room for hardware expansion. This system offers outstanding performance by virtue of an intelligent mass storage controller, intelligent streaming tape backup, high-performance system RAM and a powerful monoboard microcomputer with cache based on the MC68020 32-Bit Microprocessor. The MVME331 Serial Communications Controller and the MVME705 I/O Transition Module provides 6-channel RS-232-C serial I/O.

This modular system provides a high-performance core around which, using standard VMEmodules, a microcomputer system serving a specific application can be configured. Five additional slots in the VMEbus backplane are available for expansion. Positions are available for adding additional I/O transition modules, if desired.

For software development under the multiuser, multitasking system — SYSTEM V/68, SYS1131UY341 provides a powerful 8-user environment. Additional users can be accommodated by adding an appropriate VMEmodule such as the MVME331 Intelligent 6-Channel Serial Communication Module. The MVME320A-1 Intelligent Mass-Storage Controller supplied with the core systems enhances the use of system resources by SYSTEM V/68.

SYSTEM V/68

Derived from UNIX System V/M68000, the product jointly developed by Motorola Inc. and AT&T, SYSTEM V/68 is the validated port to the M68000 family of microprocessors. It offers a small compact kernel, which provides process scheduling and I/O facilities to all programs. Its powerful command processor, the Shell, provides for interactive control. An extensive set of tools and utilities supports program development, text processing, electronic mail and system-to-system communications. As an environment for developing application software, SYSTEM V/68 is unsurpassed.

I/Omodule, SYSTEM V/68, VMEmodule and 130bug are trademarks of Motorola Inc.
UNIX is a trademark of AT&T.
*MVMXbus is a subset of the VME Subsystem Bus

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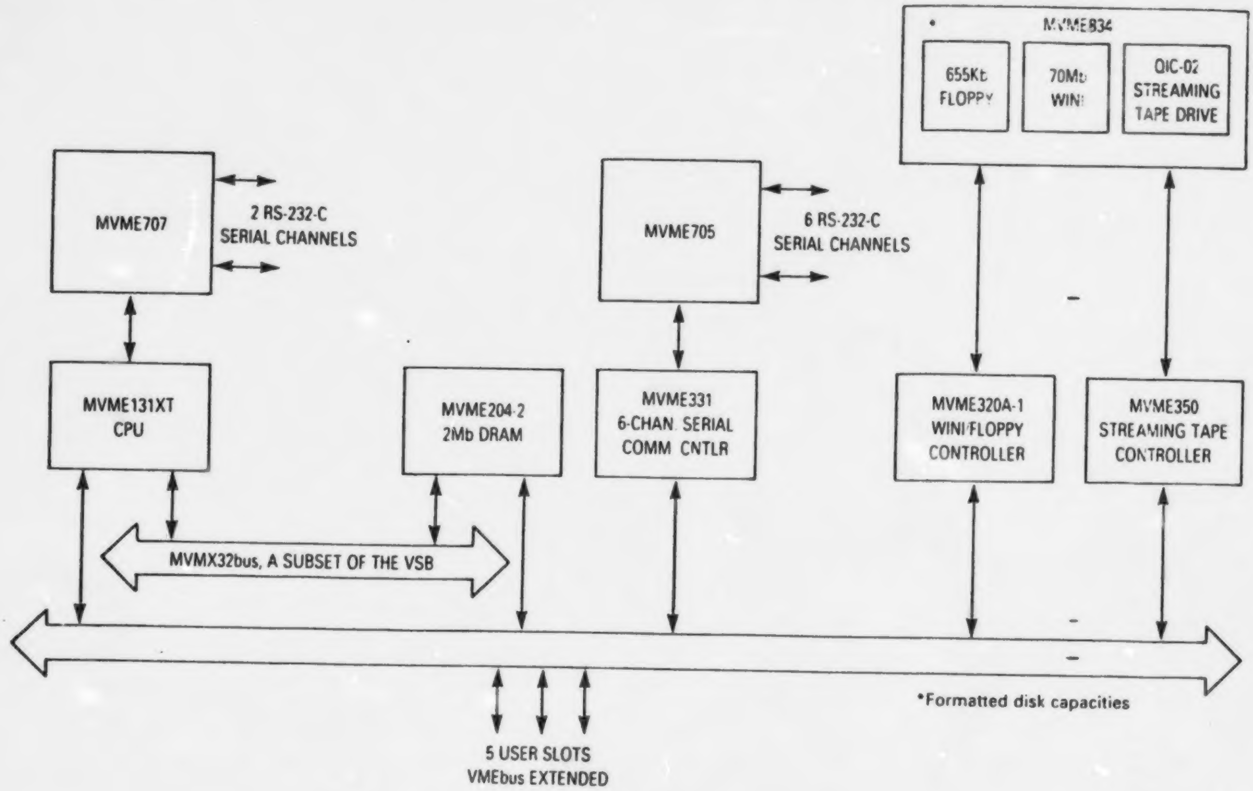
MVME834
655Kb FLOPPY
70Mb WINI
QIC-02 STREAMING TAPE DRIVE
MVME707
2 RS-232-C SERIAL CHANNELS
MVME705
6 RS-232-C SERIAL CHANNELS
MVME131XT CPU
MVME204-2 2Mb DRAM
MVME331 6-CHAN. SERIAL COMM CNTLR
MVME320A-1 WINI/FLOPPY CONTROLLER
MVME350 STREAMING TAPE CONTROLLER
MVMX32bus, A SUBSET OF THE VSB
5 USER SLOTS VMEbus EXTENDED

*Formatted disk capacities

Figure 1. SYS1131UY341 Hardware Configuration

THE SYSTEM V/68 KERNEL

The SYSTEM V/68 kernel supports a multiuser, multitasking software development and/or application execution environment. The kernel size is typically 125Kb but, depending on target system requirements, may be reduced. SYSTEM V/68 supports a layered or hierarchial file system of arbitrary size. Logical file blocks are 1024 bytes long and a hashed i-node look up feature quickens file access. The kernel is of the swapping variety. Processes may share memory segments through the optionally configurable shared memory support.

The kernel utilizes the MMB851 gate array implementation of the MC68851 Paged Memory Management Unit chip functionality to support several SYSTEM V/68 features.

HIGH LEVEL SUPPORT

Integral to SYSTEM V/68 are two categories of high level software tools which provide the means for creating, optimizing and maintaining application software. Other tools supplied with SYSTEM V/68 support text processing and communications between systems running UNIX.

Major components of the first category are the C language compiler "cc," the FORTRAN 77 compiler "f77" and the M68000/M68010/MC68020 assembler "as." Both compilers are supported by the linker/loader "ld" which supports the common object file format: COFF. Supplied also is the symbolic debugger "sdb" which can be used on C source code, FORTRAN and assembler code modules.

Software components in the second category include five editors in support of text processing under SYSTEM V/68 and two utilities supporting text formatting. The full screen editors are "ex" and "vi," "ed" is a line editor while "sed" is stream oriented and noninteractive. The editor "bfs" is a big file scanner similar to "ed."

Under SYSTEM V/68, support is also provided for electronic mail, communications and networking. By allowing a system to be used as a mail box or bulletin board, the mail utility facilitates intrasystem communications between users. Other utilities support communications with mainframe computers and networking utilities allow several computers to be linked together through dedicated links or by dial-up connections so that SYSTEM V/68 users can communicate with users on other systems running UNIX.

SYSTEMS CENTRAL PROCESSING UNIT

To provide the computing power needed to take full advantage of the vast capabilities of UNIX V, in the form of the SYSTEM V/68 Multiuser, Multitasking Operating System, a monoboard microcomputer based on the MC68020 microprocessor is used as the central processing unit by the SYS1131UY341.

Unsurpassed in its processing power, the intelligent master of this core system is an MVME131XT VMEbus Microprocessor Module featuring the state-of-the-art, full 32-bit MC68020 Microprocessor and including also MVMX32bus, a high-speed dedicated interface to the MVME204-2 2Mb Dynamic RAM, the MC68881 Floating

Point Coprocessor, a functionality subset of the MC68851 Paged Memory Management Unit implemented with gate array technology, and the Cache Accelerator, a plug-in cache memory unit designed for use with the MVME131.

The Cache Accelerator is a small, fast, static RAM system that provides concurrent, local storage of the microprocessor's VMEbus and VMX32bus memory transactions. The Cache Accelerator was designed for users wanting to accelerate the performance of their MC68020-based systems without having to modify existing programs. This software transparency feature is achieved through the utilization of a physical address cache memory structure coupled with a VME Bus Monitor.

The SYS1131UY341 system also includes an MVME707 RS-232 Serial Port Distribution Module which translates the TTL levels output by the two MVME131 ports to provide full support of RS-232-C asynchronous serial communications and which also provides two DB-25 connectors for serial I/O cables. This module is a double-high, half deep board mounted on the upper and lower rear chassis rails and connected to the MVME131XT by a 50-conductor ribbon cable.

The 130bug resident debug package (refer to Motorola publication MVME130BUG) is the firmware package designed for use with the VME131 microprocessor. 130bug provides a powerful system debugging tool for VMEmodule systems. This firmware features a one line assembler/disassembler, provisions for up/downline load, and disk bootstrap commands. 130bug is available as an EPROM-based resident package. It is plugged into IC sockets U28 and U31 on the VME131.

HARDWARE SUPPORT FOR MEMORY MANAGEMENT

Since SYSTEM V/68 utilizes memory management techniques in the manner of mainframe operating systems, hardware support for the translation of logical addresses into physical addresses and for managing the separation of user and supervisor memory spaces is essential. For the SYS1131UY341 core system, memory management support is provided by the MMB851 gate array implementation of the MC68851 Paged Memory Management Unit function.

CORE SYSTEM MAIN MEMORY

A 2Mb DRAM with parity dual-ported between VMEbus and MVMX32bus — MVME204-2 — is supplied with this core system. Up to four additional MVME204-2's can be added to this interface to provide a core system with 8Mb of high-speed memory. The base address for a module can be set on boundaries separated by the module's population.

Tailored to the MC68020 Microprocessor and specifically designed to enhance the performance of the MVME131XT VMEmodule 32-Bit Monoboard Microcomputer, the MVME204-2/MVMX32bus interface allows concurrent transfers on VMEbus with MVMX32bus transfers between the MVME131XT and MVME204-2. Implemented using high density 256K x 1-bit dynamic RAM devices, the MVME204-2 has parity generation and detection circuitry which, together with accessible control and status registers, can be used for error detection and memory diagnostics.

System memory capacity can be expanded by adding DRAM modules to VMEbus space. Use the MVME204-1, or the -2 to add 1Mb or 2Mb, respectively.

SERIAL COMMUNICATIONS CONTROLLER

The MVME331 Intelligent Communication Controller (ICC) supports six asynchronous serial communication channels at a maximum simultaneous speed of 9600 baud full duplex. The module contains a complete 16-bit microcomputer consisting of an MC68010 MPU, 128Kb RAM and firmware in two 16Kb EPROMs. This microcomputer controls three Z8530 Serial Communication Controller devices, pre-processes and transfers data between the VME system memory and the serial ports.

The transfer of commands, status messages and data packets is performed through a pipeline structure in VME system memory, which is shared between the operating system and the MVME331 firmware. This transfer follows the Buffered Pipe Protocol (BPP), a Motorola standard for processor to processor communication.

Each of the six serial channels can be configured to conform to the RS-232-C or RS-422-B standard. This is implemented on a separate Transceiver Module (MVME705 or MVME706), a double-high, half deep board mounted on the upper and lower rear chassis rails and connected to the MVME331 by a 50-conductor ribbon cable.

MASS STORAGE DEVICE CONTROLLERS

THE MVME320A-1 VMEbus DISC CONTROLLER

To control the provided floppy disk drive and Winchester disk drive, the SYS1131UY341 utilizes the MVME320A-1 VMEbus Disk Controller. Although not supported, this VMEmodule has the capability of controlling mixed 5-1/4" and 8" drives and can accommodate two 5-1/4" Winchester hard disk drives and two 5-1/4" floppy disk drives or up to four floppy disk drives.

Because the controller provides high-performance direct memory access (DMA) data channels between core system memory and the floppy and hard disk storage, the core system can be used in applications having intensive real-time disk I/O or multiprocessing structures designed to reduce VMEbus traffic and increase system throughput. Other MVME320A-1 features include:

- Supports Serial Data Rates to 5Mbps
- Supports Standard IBM Formats and MFM Recording
- 16-Bit Cyclic Redundancy Check
- 32-Bit Error Checking and Correction

THE MVME350 STREAMING TAPE CONTROLLER

A VMEmodule Intelligent Peripheral Controller (IPC), MVME350 provides control of one QIC-02 compatible, 1/4 inch streaming tape drive.

The 16Kb of static RAM onboard MVME350 provides working storage for the MC68010 vector table and stack frames. It also serves as buffer storage between the QIC-02 interface and the VMEbus. Optimum performance for typical applications is offered since the MC68010, at

10 MHz, performs zero wait state accesses of the SRAM space.

The VMEbus interface is designed to provide uniformity and compatibility among MVMEmodule drivers running under the SYSTEM V/68 as well as ease the development, by a system integrator, of software to communicate with the controller module. Controller firmware based on a multitasking kernel handles all input/output interrupts and data transfers in order to minimize impact on system throughput. Macro commands are retrieved from a pipeline structure in system memory which is shared by the MVME131XT microcomputer, and the tape controller. Status information is returned to a host through another pipeline. Exchange of command and status packets follows the Motorola buffered pipe protocol for interprocessor communication.

The following SYSTEM V/68 backup and restore utilities will be supported: finc (fast incremental backup), frec (recover file systems from a backup tape), volcopy (copy file system), cpio (copy file archives in and out) and tar (tape file archiver). In addition, the system call M350CTL will be supported to provide an application program with the means of obtaining complete control over a streaming tape device. M350CTL will support:

- Rewind Tape
- Erase Tape
- Retension Tape
- Write Filemark
- Read Filemark
- Set DMA Buffer Size
- Get DMA Buffer Size
- Byte Swapping

MASS STORAGE DEVICES

Mass storage capacity for the SYS1131UY341 system is provided by a floppy disk drive, a hard disk drive and a streaming tape.

The floppy disk is a 5-1/4" slim line drive for soft-sectored dual-sided dual-density, 96 TPI diskettes each with a capacity of 655Kb of formatted data. Features include a track density of 96 T.P.I., a recording density of 5922 B.P.I. (double density) and a data transfer rate of 250Kb per second.

The hard disk uses reliable Winchester technology and provides a capacity of 70Mb, formatted. Features include 32 sectors per track, 256 bytes per sector and a data transfer rate of 5Mb per second.

The streaming tape drive consists of a drive unit in a standard 5-1/4" half-height enclosure and a formatter/controller module which fastens to the enclosure and forms a full-height 5-1/4" product. By using the industry standard DC600 tape cartridge, a full 60Mb of tape backup can be provided.

USER INTERFACE

Starting with a suitable chassis a VMEbus-based system can be constructed from the wide variety of commercially available modules to serve almost any application. The core of this system must simultaneously offer configuration flexibility and ease of operation.

The SYS1131UY341 is housed in a MVME945 chassis assembly, the desktop decorative cover of which can be removed so that the system can be mounted in a standard 19-inch rack, if the application requires. The front of the chassis houses a card cage with backplane which accepts twelve standard double high Eurocard VMEmodules. On the right, the floppy hard disk and streaming tape drives supplied with the core system are housed in the MVME834. On the left, a power switch module is attached.

On the left in the chassis rear, attached by screws to the upper and lower rails, are the two 80 mm I/O Transition Modules supplied with the SYS1131UY341. The remaining space can be used for additional transition modules.

A 400 watt power supply is mounted in a fan-cooled air duct assembly located in the upper half of the chassis to the rear of the VMEmodule backplane. Additional cooling sufficient for an expanded system is provided in the chassis.

By virtue of the high intelligence and integration levels of its modules, the SYS1131UY341 is able to present to the user an uncluttered front which offers the essential basic controls and system status indications and, at the same time, the means of configuring the hardware to provide certain system level functions.

MVME131XT Front Panel —
FAIL Indicator, Red LED
HALT Indicator, Red LED
RUN Indicator, Green LED
SCON Indicator, Green LED
Reset Switch, spring-loaded pushbutton
Abort Switch, spring-loaded pushbutton
8-Position DIP Switch
50-Pin Connector
RUN Indicator, cache module, Green LED

MVME204-2 Front Panel —
Power Indicator, Green LED

MVME320A-1 Front Panel
FAIL Indicator, Red LED
Two Slots for ribbon cable entry/exit

MVME350 Front Panel
FAIL Indicator, Red LED
HALT Indicator, Red LED
RUN Indicator, Green LED

EXPANSION FOR ADDITIONAL USERS

The backplane supplied with the SYS1131UY341 chassis can accommodate additional VMEmodules. Access to the unused slots is gained by removing the screws fastening dummy module front panels to the upper and lower rails of the chassis front.

The eight serial interfaces provided with this core system for terminals or other I/O devices can be expanded by six RS-232-C or RS-422-B ports by installing the MVME331 Intelligent Communications Controller Module in the chassis backplane. A companion I/O Transition Module, the MVME705 which supplies the DB-25 connectors and the transmitters/receivers required to support the two communication protocols is installed by screwing the module front panel to the top and bottom rear rails of the chassis. Connection is made between the two modules using a 64-conductor ribbon cable.

Memory can be supplemented in increments of 1 or 2 megabytes by adding the MVME204-1 or -2.

Extensive documentation for the hardware and SYSTEM V/68 is supplied with the SYS1131UY341. Documentation supplied for SYSTEM V/68 describes in detail the process of generating a new kernel for use with an expanded system. Hardware and module documentation supplied with the core system and expansion modules details the process of configuring a system to comply with the requirements of various applications.

SYS1131UY341 SYSTEM TEST

The SYS1131UY341 System Test is a comprehensive set of powerful system level tests and fault isolation diagnostics. The software executes on this VMEbus Modular System with SYSTEM V/68 or on other VMEbus hosts and can be a versatile tool for system operators, as well as engineering, manufacturing and field service personnel. It can be used for new design verification, for system product verification or for performance measurement and fault isolation in installed systems. It can also serve the system integrator as the basic test structure in which tests for added modules can be included as a means of offering a system test facility with the custom configuration.

SYS1131UY341 System Test features include:

- Simple Default Mode — Test of the as-shipped SYS1131UY341 VMEbus Modular System
- Flexible, easy-to-use Operator Interface Accommodates Varying Needs:
  - — Change complement of tests for a new system configuration
  - — Change sequence of tests to provide a new test environment
  - — Change internal execution of a test to meet specific requirements
- Elaborate Test Environment Controls for Fault Isolation
- Timer Functions to Support System Performance Measurement
- Error Logger and I/O Re-direction for Test Record Keeping
- Extensive Manual Debugger for Fault Isolation and Specific Function Checks
- Target Environment Simulated by Tasks Executing Under a Real-Time, Multitasking Kernel
- C Language Source Available for Straightforward Porting

To provide the essential synchronizing functions and task control utilities required for the simulation of a target operating system, SYS1131UY341 System Test utilizes a real-time, multitasking kernel. This allows multiple test tasks to execute concurrently creating a realistic on-line simulation in a controlled environment. Use of a real-time, multitasking kernel also facilitated the creation of utilities for dynamically tailoring test conditions to match changing hardware configurations and for pinpointing a specific fault or measurement state. The addition of a multi-faceted debug utility resulted in a system test capability that isolates faults to the replaceable component level — and beyond.

VMEbus

Rapidly becoming the leading bus standard in U.S., European and other world markets, VMEbus is a 8-/16-/32-bit interconnect that has a master/slave asynchronous, non-multiplexed data transfer structure, seven levels of priority interrupt, four levels of data bus arbitration, multiple master support, fault detection and control, and special transfer cycles.

The VMEbus functional structure consists of backplane interface logic, four groups of signal lines called buses each having its own collection of functional modules any number of which can be grouped on a board and which communicate with the other functional modules of a bus via onboard or backplane signal lines.

The VMEbus mechanical structure comprises subracks, backplanes, front panels, plug-in boards and other elements all of which conform to relevant IEC Eurocard specifications to insure that all components fit together properly.

These features combined with reliability, mechanical integrity, 20 megabytes-per-second performance and the fact that it is nonproprietary have resulted in almost complete acceptance of VMEbus by the electronics industry. Currently over 200 vendors are manufacturing over 1000 VMEsystem-compatible products, assuring for the expansion of a core system, the widest selection of functions from the greatest number of sources so that the broadest range of applications can be served.

ORDERING INFORMATION

Part Number	Description
SYS1131UY341	VMEbus Modular System with SYSTEM V/68, includes: MVME131XT VMEmodule Monoboard Microcomputer with cache MVME204-2 2Mb Dual-Ported DRAM MVME320A-1 VMEbus Disk Drive Controller MVME331 Serial Communications Controller MVME350 Streaming Tape Controller MVME705 Transition Module MVME 707 Transition Module MVME834 Plug-In Mass Storage Module with — 70Mb Winchester Disk Drive — 655Kb Floppy Disk Drive — Streaming Cartridge Tape Drive MVME945 VMEbus Chassis Assembly with — 32-Bit VMEbus Backplane — 400 W Power Supply User's Manuals for SYSTEM V/68, chassis and all modules included

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

MVME1131UY341	
MCU	MVME131XT VMEmodule 32-Bit Address/Data Monoboard Microcomputer (16.67 MHz MC68020 Microprocessor, 16Kb Physical Cache Memory and MC68881 FPCP)
Memory	2Mb Dual-Ported RAM with MVMX32bus (MVME204-2)
Mass Storage Controllers	MVME320A-1 VMEbus Disk Controller MVME350 VMEbus Streaming Tape Controller
Serial I/O Controller	MVME331 Serial Communications Controller
Mass Storage	70Mb (formatted) Winchester Disk Drive 655Kb (formatted) Floppy Disk Drive Streaming Cartridge Tape Drive
I/O Interfaces	8 x RS-232-C programmable to 19.2K baud Rear serial I/O connections via MVME705 & MVME707 Transition Modules
Expansion Slots	12-slot Backplane, 5 slots free for user
Power Supply	400 W (115 Vac)
Operating Temperature	5° to 40° inlet air temperature, forced air cooling
Operating Humidity	20% to 80% (non-condensing)

OPTIONS

Part Number	Description
MVME204-1,-2	1Mb/2Mb Interleaved Dual-Ported DRAM Modules
MVME214	A32/D32 Static RAM/ROM Memory Module
MVME331,332	6-/8-Channel Intelligent Communications Controllers
MVME705, 706	I/O Transition Boards for MVME331

RELATED DOCUMENTATION

Part Number	Description
MVMESYSAM/D	VME System Architecture Guide
MC68020/D	MC68020 Microprocessor User's Manual
HB212/D	VMEbus Specification Manual

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Power Supply	400 W (115 Vac)
Operating Temperature	5° to 40° inlet air temperature, forced air cooling
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OPTIONS

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MVME214	A32/D32 Static RAM/ROM Memory Module
MVME331,332	6-/8-Channel Intelligent Communications Controllers
MVME705, 706	I/O Transition Boards for MVME331

RELATED DOCUMENTATION

Part Number	Description
MVMESYSAM/D	VME System Architecture Guide
MC68020/D	MC68020 Microprocessor User's Manual
HB212/D	VMEbus Specification Manual

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MICROSYSTEMS PRODUCTS
TECHNICAL DATA

Order this data sheet
by MVME945-1/DD

MVME945-1
MVME945-2
MVME833
MVME834
ACCESSORIES

VMEbus Chassis Assembly, Mass Storage Modules and Accessories

MVME945 CHASSIS FEATURES

- Internationally Approved (UL, CSA, VDE) 400 Watt Power Supply
  - — Jumper-selectable 115/230 Vac input
  - — Short circuit protection
  - — Over-voltage protection
  - — Remote sensing for accurate module voltage
- 12-Slot, 32-Bit, VMEbus Compatible Backplane
  - — Provides all signal/power line connections for full 32-bit operation
  - — Jumper areas for daisy-chain signals
  - — Bus terminators provided
- 19-inch Rack-mountable Chassis
- Forced Air Cooling for Power Supply, Mass Storage Modules and VMEmodules
- Rear Mounted Card Cage for Up To 21–700 Series Transition Modules
- ESD Hardening and Electromagnetic Interference (EMI) Shielding (FCC and VDE Compliant)
- Meets UL, VDE and CSA Safety Requirements

MVME833 FEATURES

- 70Mb (formatted) 5-1/4" Full-High Winchester Disk Drive, ST506 Compatible
- 655Kb (formatted) 5-1/4" Double-Sided, Double-Density, Half-High Floppy Disk Drive, SA400 Compatible

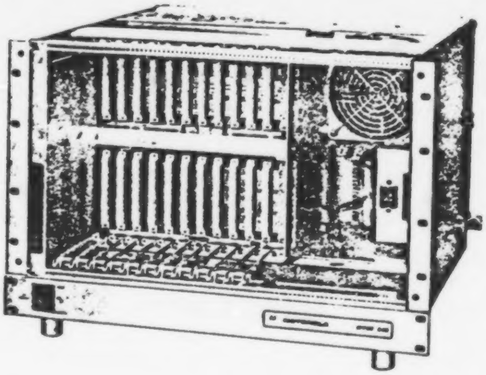
MVME834 FEATURES

- 70Mb (formatted) 5-1/4" Full-High Winchester Disk Drive, ST506 Compatible
- 655Kb (formatted) 5-1/4" Double-Sided, Double-Density, Half-High Floppy Disk Drive, SA400 Compatible
- QIC-02 Compatible Streaming Tape Drive. Accepts ANSI Standard X3.55-1982 1/4" Tape Cartridges

ACCESSORIES

- MVME945CNVKT — 115 Vac to 230 Vac Conversion Kit
- MVME945I/O — I/O Channel Card Cage Kit
- MVME945CVR — Desk Top Cover for MVME945
- MVME83XKT — Mass Storage Expansion Kit
- MVME83XSTKT — Streaming Tape Expansion Kit

MVME945 CHASSIS ASSEMBLY



The MVME345 chassis is designed to help convert individual VMEmodule board-level products into a complete, compact, self-contained microcomputer system. This packaging design helps to best meet the user's specific performance and installation requirements. Various options permit the convenient assembly of systems for custom installations/applications.

The following paragraphs present an overview of the MVME945 chassis and its major assemblies and/or components.

CHASSIS

The MVME945 chassis is 19" wide, 19-3/4" deep, and 12-1/4" high. It houses a VMEmodule card cage with 12 VMEbus slots. It has a front panel opening for the MVME83x series of mass storage modules. An ON/OFF power switch is located on the lower, left front and a fuse assembly is located on the lower, left rear. Power is supplied by an internal 400 watt power supply, which is mounted in the upper half, and toward the rear of the chassis. There are provisions for 21 rear panel mounted 80 mm interface modules (MVME7xx).

Three dc-powered fans provide forced air cooling for the power supply, mass storage enclosure and VMEmodules. Convection cooling is used for the MVME7xx series modules.

Double-high 80 mm modules such as Motorola's MVME7xx series modules can be mounted in the rear of the chassis, although no power or support is provided. Alternatively, additional Eurocard chassis rails and backplanes for single-high I/O Channel modules can be installed in this area. Nine I/O modules can be used in the MVME945 chassis when the optional I/O Channel kit (MVME945I/O) is installed.

The MVME945 specifications are shown in Table 1.

VMEmodule is a trademark of Motorola Inc.

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Table 1. MVME945 Chassis Specifications

Characteristics	Specifications
Dimensions Width (with front flange) (without front flange) Depth Height	 19 in. (482.6 mm) 17.2 in. (436.8 mm) 19.75 in. (501.7 mm) 12.2 in. (266.7 mm)
Weight	TBD
Input Voltage	90 Vac to 132 Vac or 180 Vac to 264 Vac
Input Frequency	47 Hz to 63 Hz
Input Power	575 VA (max)
Output Voltages	+5 Vdc @ 50 A (max) +12 Vdc @ 10 A (max) −12 Vdc @ 5 A (max)
Output Power	400 Watts (max)
Temperature* Operating Storage	 +5°C to +40°C −30°C to +60°C
Relative Humidity*	20% to 80% (non-condensing)
Altitude	10,000 ft.

*These are generic limitations imposed by the MVME83X Mass Storage Modules. Broader limits are possible if peripherals are not mounted in the MVME945, or if more tolerant peripherals are selected, or if more powerful fans are used.

POWER SUPPLY

DC power for the backplane, optional disk drives and all VMEmodules is supplied by a UL, CSA, VDE certified 400 Watt power supply. This supply is easily converted from 115 Vac to 230 Vac operation by installing the MVME945CNVKT (115 Vac to 230 Vac) conversion kit, and provides overvoltage protection for the +5 Vdc output. This power supply is mounted in the fan-cooled air duct assembly, located in the upper half of the chassis behind the backplane for ease of servicing. The air duct also provides EMI/RFI shielding for the power supply.

Several different power supplies may be qualified for use in the MVME945 chassis, each of which may have slightly different specifications. For this reason, the power supply specifications shown in Table 2 should be considered approximate, with the possibility of some variation.

VMEbus BACKPLANE

The MVME945 chassis contains one 12 slot, full 32-bit VMEbus backplane mounted to the left of the optional mass storage area. This backplane contains 12 connectors (sockets) on the top row to receive connector P1 of the VMEbus and another 12 connectors on the bottom row to receive P2 of the VMEbus. All rows of P1 (A, B, C) are interconnected across all 12 slots providing the required signals for A24/D16 operation and the center row (B) of P2 is interconnected across all 12 slots providing the required signals for extended operation (A32/D32). Rows A and C of P2 are not interconnected, but are left available to the user for I/O or expansion bus operation.

To manage signal reflections and provide noise margin, all signal lines not daisy-chained are terminated with 470 Ω (pull-down) and 330 Ω (pull-up) resistors. These resistors are arranged in networks and are permanently installed on the rear outer edges of the backplane board adjacent to the P1 and P2 connectors.

The terminators are also intended to provide "active negative spike suppression" for the SYSCLK and SERCLK signal lines.

The +5 Vdc power lines (input from power supply) are connected to the backplane through ring lugs and #10 studs at the center of the backplane. The +12 Vdc, −12 Vdc and +5 Vdc sense power lines are connected to the backplane through a 5-position "mate-n-lok" connector. These connectors are rated at 60 A for the +5 Vdc lines and 10 A for the +12 Vdc and −12 Vdc

Table 2a. Power Supply Specifications

Characteristics	Specifications
Output Ripple and Noise Ripple Noise	 1% peak-to-peak or 100 mV, whichever is greater 0.2% V_{rms}
Holdover Storage	16 ms/min at Vac = 115 and rated power
Overload Protection	All outputs are protected against damage from overloads and shorts.
Rated Output Power	400 Watts (max)
Output Ratings Minimum Load Operation	 5 A on the +5 Vdc Output

Table 2b. Power Supply Output

Output Number	DC Voltage	Current Amp(s)	Load Reg. (20% to 100% change)	Line Reg. (Low Vac to High Vac)	Cross Reg. (35% to 85% Change on Output #1)
1	+5	50	+1%	+0.2%	+1%
2	+12	10	Must stay within +5% for any combination of line, load, cross regulation and centering.		
3	−12	5			

lines. A 2-position "mate-n-lok" connector provides a +5 Vdc standby power source to the backplane. This connector is rated at 2 A.

Four 5-position "mate-n-lok" "output" connectors are provided for distributing dc power to peripheral devices, such as disk drives and fans. They provide distribution for +5 Vdc, +12 Vdc and −12 Vdc and are rated at 5 A. Also, a 4-position connector provides power for dc status indicator lamps. This connector distributes +5 Vdc, +12 Vdc and −12 Vdc at 100 mA.

The backplane specifications are shown in Table 3.

Table 3. VMEbus Backplane Specifications

Characteristics	Specifications
Dimensions Width Height	 10.10 in. (256.54 mm) 10.31 in. (261.87 mm)
Power Consumption	6 Watts (1.2 A @ +5 Vdc) (Required by terminator networks)
VMEbus Connectors	24 sockets: DIN 41612, Type C, 96-pin Socket spacing (center-to-center) = 0.8 inches
Power Connectors	INPUT Voltage / Current / Connector +5 Vdc / 60 A / #10 studs +5 Vdc Sense / — / mate-n-lok 5-position +12 Vdc / 10 A / −12 Vdc / 10 A / +5 Vdc Stby / 2 A / mate-n-lok 2-position OUTPUT Voltage / Current / Connector +5 Vdc / 5 A / mate-n-lok 5-position +12 Vdc / 5 A / −12 Vdc / 5 A / +5 Vdc / 100 mA / Amp 4-position +12 Vdc / 100 mA / −12 Vdc / 100 mA /
VMEbus Headers	Headers provided on front and rear of backplane for daisy-chain of VMEbus signals.
Bus Termination	Signal lines are terminated with 330 Ω pull-up resistors and 470 Ω pull-down resistors. SYSCLK and SERCLK signal lines have clamp diodes for negative spike suppression.

FCC AND VDE COMPLIANCE

The Federal Communications Commission (FCC) has established technical standards regarding radiation and conduction of EMI and Radio Frequency Interference. The MVME945 chassis has been tested with Motorola VMEmodules and mass storage enclosures and found to comply with the emission limits for a class A computing device in accordance with the specifications of the FCC and VDE regulations. Compliance was achieved under the following conditions:

a) The chassis was connected to earth ground through the safety ground wire in the power cord. This provided the path for connecting shields to earth ground.

b) All external I/O cables were high quality shielded types with metal shell connectors. External I/O connectors on VMEmodules were metal shell types connected to chassis ground. This was accomplished through the conductive panels in contact with the chassis rails. VMEmodules must have conductive panels to ensure a good RF ground with the conductive chassis rails.

c) Blank panels were installed to cover all unused chassis slots to minimize RF leaks in the chassis.

d) Front panel screws were properly tightened for good grounding.

e) The desk top cover was installed. (If the MVME945 is rack mounted, the system integrator must ensure that the system remains compliant.)

For minimum RF emissions, it is essential that the foregoing conditions be implemented. Failure to do so could compromise the FCC or VDE compliance of the system.

In addition to meeting the FCC and VDE emission standards, the MVME945 meets all UL, VDE and CSA safety requirements.

CHASSIS COOLING CONSIDERATIONS

The MVME945 chassis provides forced air cooling for the standard VMEmodules, mass storage modules and power supply. The VMEmodules are cooled by air which is drawn into the bottom of the chassis by two low noise, 70 CFM, dc fans, forced past the VMEmodules, and blown out the top of the chassis. These fans provide air flow which is sufficient for most VMEmodules. Certain high density, high power modules, when used at elevated temperatures may require additional cooling. When possible, high power modules should be distributed throughout the chassis to reduce "hot spots." Also, the 70 CFM fans can be replaced by 100 CFM fans to improve air flow, but, at the expense of higher acoustic noise. The system integrator must ensure that adequate cooling is provided for all modules used in the system.

The mass storage enclosure and power supply are cooled by air which is drawn into the mass storage enclosure by a low noise, 70 CFM, dc fan and then forced past the power supply and out the left side of the chassis.

No forced air cooling is provided for the rear mounted MVME7xx series modules and optional I/O Channel card cage. The MVME7xx series modules are typically transition modules with few active components, and cooling is generally not required. Many I/O Channel modules are low power, low density designs that will be cooled adequately by convection. Thus, such modules normally do not require forced air cooling. However, if the MVME945 chassis is used at high temperatures (greater than 25°C), with the optional I/O Channel card cage and high power I/O Channel modules installed, forced air cooling for the I/O Channel modules might be required. The system integrator must ensure that adequate cooling is provided.

General Cooling Precautions

a) Ensure the air space above and below the chassis is not blocked, and the inlet screens are clean.

b) Air inlet temperature must not exceed 40°C.

c) All unused VMEmodule slots must be covered to prevent cooling air from escaping the chassis.

d) Chassis should be used only in a clean environment.

CAUTION: If the MVME945 is installed in a rack with other chassis, be sure each chassis in the rack is provided with its own supply of fresh outside cooling air.

MVME83x MASS STORAGE ASSEMBLIES

The MVME83x series assemblies provide mass storage for Motorola VMEsystems. They slide directly into the right front side of an MVME945 chassis and are connected by cable to the MVME320A-1 and MVME350 controller boards (Not included with the Mass Storage Assemblies). A support frame which slides into four heavy duty VMEmodule card guides and is retained in place by four captive screws on the front panel is used for mounting an assembly. Major components of the MVME83x series assemblies are described in the following paragraphs.

WINCHESTER HARD DISK (MVME833/MVME834)

The Winchester disk supplied with the MVME833 and MVME834 Plug-in Mass Storage Modules will be a Micropolis 1320 series, a Toshiba MK-56 series, or similar-type drive. Both of these drives utilize a Winchester-type head/media technology and provide both dc operating voltages and outline dimensions consistent with the industry-standard. The specifications for the Micropolis 1320 series are shown in Table 4 and the specifications for the Toshiba MK-56 are shown in Table 5. Should a different Winchester hard disk drive be utilized in the MVME833/MVME834, the specifications may not be identical to those shown.

Table 4. Micropolis 1320 Specifications

Characteristics	Specifications		
Capacity			
Unformatted			
Per Drive (Mb)	85.30		
Per Surface (Mb)	10.70		
Per Track (Bytes)	10,416		
Formatted*			
Per Drive (Mb)	67.10		
Per Surface (Mb)	8.39		
Per Track (Bytes)	8,192		
Per Sector (Mb)	256		
Sectors/Track	32		
Cylinders	1,024		
Read/Write Heads	8		
Pre Comp Cylinder	DO NOT USE		
Seek Time (includes settling)			
Track-to-Track (ms)	6		
Average (ms)	28		
Maximum (ms)	62		
Latency Time (avg)(ms)	8.33		
Power Requirements	Idle	Seeking	Peak
+5 Vdc +5%	0.9 A	0.9 A	0.9 A
+12 Vdc +5%	2.1 A	3.3 A	3.9 A
Power Dissipation	28 W	38 W	

*Assumes format compatible with Motorola OS.

Table 5. Toshiba MK-56FB Specifications

Characteristics	Specifications
Capacity	
Unformatted	
Per Drive (Mb)	86.50
Per Surface (Mb)	8.64
Per Track (Bytes)	10,416
Formatted*	
Per Drive (Mb)	68
Per Surface (Mb)	6.80
Per Track (Bytes)	8,192
Per Sector (Mb)	256
Sectors/Track	32
Cylinders	830
Read/Write Heads	10
Pre Comp Cylinder	512
Seek Time (includes settling)	
Track-to-Track (ms)	6
Average (ms)	25
Maximum (ms)	45
Latency Time (avg)(ms)	8.33
Power Requirements	1.3 A max 0.09 A typ
+5 Vdc +5%	Seeking 4.2 A max 10 ms
+12 Vdc +5%	PK Starting 3.8 A max
	120 sec
	Idle 1.5 A
Power Dissipation	30 W nom

*Assumes format compatible with Motorola OS.

FLOPPY DISK (MVME833/MVME834)

The floppy disk supplied with the MVME833/MVME834 Plug-In Mass Storage Modules is an industry standard 5-1/4", half height (1.63"), soft sector, FM/MFM mini-flexible disk drive. Several manufacturers' drives are qualified to be used in the MVME833/MVME834 and the specifications shown in Table 6 are generic to those manufacturers.

Table 6. Floppy Disk Specifications

Characteristics	Specifications
Capacity	
Unformatted	
Per Drive (Mb)	1
Per Surface (Mb)	0.5
Per Track (Bytes)	12,500
Formatted*	
Per Drive (Mb)	0.655
Per Surface (Mb)	0.3277
Per Track (Bytes)	8,192
Per Sector (Mb)	256
Sectors/Track	32
Cylinders	40
Read/Write Heads	2
Pre Comp Cylinder	NOT REQUIRED
Seek Time (includes settling)	
Track-to-Track (ms)	18
Average (ms)	109
Maximum (ms)	62
Head Settle Time (ms)	15
Latency Time (avg)(ms)	10
Power Requirements	
+5 Vdc +5%	0.3 A typ 0.38 A max
+12 Vdc +5%	0.22 A typ 0.54 A max
Power Dissipation	6 W

*Assumes format compatible with Motorola OS.

STREAMING TAPE DRIVE (MVME834 ONLY)

The streaming tape drive supplied with the MVME834 Plug-In Mass Storage Module will be the Archive Corp. model 5945L3 or similar type drive, a 9-track half-height drive capable of streaming or start/stop operation with data capacities of 30Mb or 60Mb when used with the DC 300XL or DC 600XL cartridges respectively. Also included is a formatter/controller for a QIC-02 interface which, when integrated with the drive results in a full height 5-1/4" module. Specifications for the 5945L3 are shown in Tables 7 and 8. Should a different streaming tape drive be used in the MVME834, the specifications may not be identical to those shown.

MVME833/MVME834 CABLING

The MVME833 and MVME834 are provided with the cabling required to interface directly to a series of Motorola mass storage controllers. The Winchester and floppy disk drives directly interface the MVME320A or MVME320A-1, and the streaming tape drive connects directly to the MVME350. Cabling instructions are provided in the MVME833 and MVME834 manuals.

Table 7. Archive 5945L3 Specifications

Characteristics	Specifications
No. of Tracks	9
No. of Channels*	2
Capacity — DC 300XL	30Mb
Capacity — DC 600XL	60Mb
Backup Time — DC 300XL	9 min
Backup Time — DC 600XL	12 min
Recording Mode	NRZI
Recording Data Density	8000 bpi
Encoding Method	4 to 5 RLL**
Track Capacity — DC 300XL	5Mb
Track Capacity — DC 600XL	6.6Mb
Data Transfer Speed	90Kb/s
Tape Speed	90 ips
Start/Stop Time	300 ms max

ACCESSORIES

MVME945I/O — This kit provides the hardware required to add 9-slots of I/O Channel expansion capability to the MVME945 chassis. Included is the I/O Channel card cage, backplanes and interconnection cable to attach directly to a P2 connector of the 12-slot VMEbus backplane. When assembled and installed in the rear of the MVME945 chassis, the I/O Channel expansion kit occupies 11 of the MVME7xx transition module slots, leaving 10 for transition module requirements.

For I/O Channel operation, an I/O Channel master VMEmodule such as the MVME110-1 or MVME316 (not included in the kit) is required.

MVME945CNVKT — This kit provides the material required to convert the MVME945 from 115 Vac operation to 230 Vac operation. Included are 230 Vac rating labels, 2 fuses and detailed instructions for the conversion process.

MVME945CVR — This kit provides the desk top cover and attachment hardware for the MVME945 chassis. The cover is designed to provide FCC and VDE compliance but cannot be used when the chassis is rack mounted.

MVME83XKT — This kit provides the metal work used in the MVME83x series mass storage modules. The frame is capable of accepting 2 full-height and 1 half-height, 5-1/4" mass storage modules, and gives the system integrator the ability to construct a custom mass storage module to meet his own application requirements. No drives or cables are supplied, but detailed instructions are provided for assembly as well as examples of how to install and cable various mass storage modules.

MVME83XSTKT — This kit provides all the necessary material to convert an MVME833 to an MVME834. Included is the required metal work, hardware, streaming tape drive and cables. The streaming tape controller board (MVME350) is not included and should be ordered separately.

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Table 8. Archive 5945L3 Power Specifications

DC Voltage	+12 Vdc	+5 Vdc
Tolerance (includes 200 mv max ripple)	+10%	+10%
Operational Current	1.75 A +0.8 (cartridge dependent)	2.4 A max
Tape Start or Stop Surge Current Peak	4.15 A max up to 300 ms	0.0 A
Power On Surge Current	Thru 200 μF max cap	Thru 60 μF max cap
Voltage Rise Time	100 ms max	100 ms max
Power Sequence	None	None
Power Dissipation (in continuous streaming mode)	21 Watts	12 Watts
Power Dissipation (during start or stop power surges)	50 Watts	12 Watts

ORDERING INFORMATION

Part Number	Description
MVME945-1	VME Chassis Assembly with 12-slot Backplane, 400 W Power Supply and provision for mass storage modules. Operates at 115 Vac. Includes User's Manual.
MVME945-2	VME Chassis Assembly with 12-slot Backplane, 400 W Power Supply and provision for mass storage modules. Operates at 230 Vac. Includes User's Manual.
MVME833	Plug-In Mass Storage Unit for use with MVME945 — Includes 70Mb Winchester 655Kb Floppy and all required cables. Includes User's Manual.
MVME834	Plug-In Mass Storage Unit for use with MVME945 — Includes 70Mb Winchester 655Kb Floppy, Streaming Tape and all required cables. Includes User's Manual.
MVME945I/O	I/O Channel Expansion Kit. Includes installation instructions.
MVME945CNVKT	115 Vac to 230 Vac Conversion Kit. Includes installation instructions.
MVME945CVR	Desk Top Cover for MVME945. Includes installation instructions.
MVME83XKT	Custom Mass Storage Expansion Kit. Includes installation instructions.
MVME83XSTKT	Streaming Tape Upgrade Kit for MVME833. Includes installation instructions.

RELATED DOCUMENTATION

Part Number	Description
MVME945/D	MVME945 Chassis User's Manual.
MVME830/D	MVME833/MVME834 Plug-In Mass Storage User's Manual.
MVME945IO/D	MVME945 I/O Channel Expansion Kit Installation Instructions.
MVME945CP/D	MVME945 115 Vac to 230 Vac Conversion Kit Installation Instructions.
MVME945CVR/D	MVME945 Desk Top Cover Installation Instructions.
MVME83XKT/D	MVME83x Custom Mass Storage Expansion Kit Installation Instructions.
MVME834UP/D	MVME833 Streaming Tape Upgrade Kit Installation Instructions.
MVME320A/D	VMEbus Disk Controller Module User's Manual.
MVME350/D	VMEbus Streaming Tape Controller User's Manual.

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MOTOROLA

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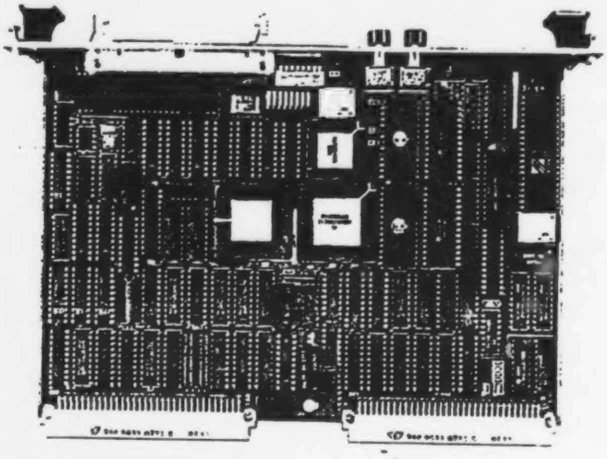
MVME130
MVME131

VMEmodule 32-Bit Monoboard Microcomputer



The VMEmodule 32-bit Monoboard Microcomputer (MVME130) is designed to function in those applications requiring maximum performance while maintaining the versatility inherent in VMEmodule systems. Highest performance is attained when the MVME130 is used in conjunction with one or more MVME204 Dual Ported RAM Cards operating as a main memory. The MVME130 is the first VMEmodule product to offer the following:

- MC68020 Microprocessor with 32-bit Address and Data VMEbus Interface
- Provision for MC68881 Floating Point Coprocessor (customer-supplied option)
- Provision for Demand Paged Virtual Memory Management Board (MMB) Implemented with Gate Array Technology
- Two 28-pin JEDEC Sockets for up to 16Kb Onboard Static RAM
- MVMX32bus* Interface Provides High-speed Data Path to/from Memory
- VMEbus Interface Allows User Configuration of Microcomputer System to Fit the Application
- VMEbus Interrupter, Interrupt Handler, and Arbiter Onboard
- Programmable Timer Module
- Dual Multiprotocol Serial I/O Ports
- Accepts MVME130bug Debug Monitor Firmware (optionally available)
- Two ROM Sockets Configured for Industry Standard 28-Pin ROM/EPROM devices. Four ROM Sockets Available when no Sockets are Devoted to RAM
- Broadcast Interrupt Capability for Multi-processor Synchronizing Applications

CPU

The MVME130 uses an MC68020 Microprocessor operating at a fixed speed of 12.5 MHz. This CPU will eventually operate at 16.67 MHz on the MVME130. The MC68020 is the first product within the popular MC68000 family to offer external 32-bit address and data paths. With its higher clock rate, advanced architecture, enhanced addressing modes, and on-chip instruction cache, this product offers state-of-the-art performance while maintaining software compatibility with its widely accepted predecessors.

DEBUG MONITOR FIRMWARE

The MVME130bug Debug Monitor firmware package is optionally available for use with the MVME130 module. This firmware offers 32 debug, up/downline load, one line assembler/disassembler and disk bootstrap load commands.

COPROCESSOR

The MVME130 module is equipped with a socket to accept the MC68881 Floating Point Coprocessor, a customer supplied option. When available and installed, the MC68881 Floating Point Coprocessor will improve computing speed of the MVME130 when the system is utilized in applications requiring arithmetic operations.

The MVME130 utilizes the MC68020 Coprocessor Interface to provide a logical extension to the MC68020 architecture and instruction set.

Figure 1 is a block diagram of the MVME130 module.

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*MVMX32bus is a Motorola Proprietary Expansion bus for use with VMEbus.
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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1164
(Replaces NP177)
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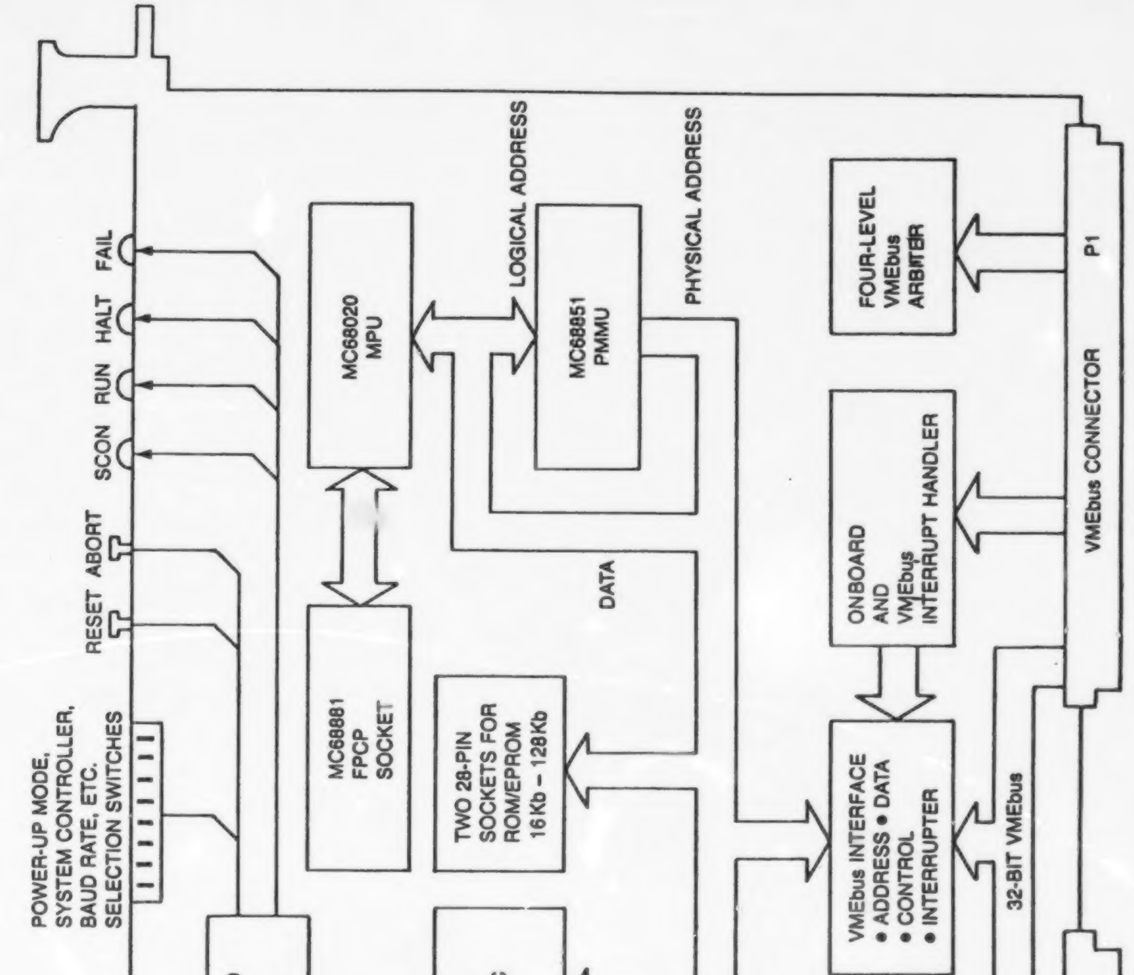
FIGURE 1 — MVME130 32-Bit Microcomputer Module


50-PIN RIBBON CABLE CONNECTOR — TTL TO EXTERNAL RS-232C TRANSITION MODULE
POWER-UP MODE, SYSTEM CONTROLLER, BAUD RATE, ETC. SELECTION SWITCHES
RESET
ABORT
SCON
RUN
HALT
FAIL
MK68564 TWO MULTIPROTOCOL SERIAL PORTS
STATUS AND CONTROL REGISTERS
MC68881 FPCP SOCKET
MC68020 MPU
LOGICAL ADDRESS
MC68851 PMMU
PHYSICAL ADDRESS
16Kb STATIC RAM
TWO 28-PIN SOCKETS FOR ROM/EPROM 16Kb – 128Kb
DATA
MVMX32bus INTERFACE
THREE 78036A 16-BIT TIMERS
VMEbus INTERFACE
• ADDRESS • DATA
• CONTROL
• INTERRUPTER
ONBOARD AND VMEbus INTERRUPT HANDLER
FOUR-LEVEL VMEbus ARBITER
32-BIT VMEbus
P2
VMEbus CONNECTOR
P1

MVME130
MVME131

MEMORY MANAGEMENT

The MVME130 is designed to eventually utilize the MC68851 Demand Paged Virtual Memory Management Unit. However, one initial version of the MVME130 (MVME131) utilizes a Memory Management Board (MMB) which conforms to a subset of the MC68851. This subset is implemented via gate array technology together with other semiconductor devices mounted on a secondary PC board. The socket assigned for future use with the MC68851 is utilized to mount the secondary PC board in a mezzanine fashion on the introductory version of the MVME130. The MMB offers the following features:

- Logical address consisting of:
  - — 32-bit Address
  - — 3-bit Function Code
- Physical address output of 32 bits.
- Logical to physical address translation;
  - — Table walking algorithm
  - — Single logical bus master
  - — Single page size (1Kb)
- Used, modified, and write protect bits.
- Supports MC68020 and external data cache.
- 512 entry set associative cache.

The eventual use of the MC68851 will add multiple Protection/Privilege capabilities.

The principal operating function of the MMB on the MVME130 is to provide the hardware logical to physical address translation and access protection necessary for operating system support. The MMB logical to physical translation mapping function utilizes a table-walking algorithmic search through memory-resident translation tables. The MMB utilizes a cache architecture to eliminate table-walking for most CPU bus cycles.

The MMB utilizes the MC68020 clock circuitry, but does not use the coprocessor interface. This requires the internal registers to be in the CPU address space, whereas the MC68851 internal registers will be accessed via the coprocessor interface. This will require a change in driver routines when the MC68851 is used with the MVME130.

ONBOARD STATIC RAM

The MVME130 Static Memory is implemented with two 28-pin industry-standard JEDEC sockets. The MVME130 will provide 16Kb of single-ported memory for the MC68020 local processor. However, if the user does not require the onboard memory, the two static RAM sockets can be reconfigured to accept EPROMS up to 512K in size.

MVMX32bus INTERFACE

The MVMX32bus Interface occupies 64 P2 I/O pins and is designed to serve as the system's high-speed memory access channel. The signals utilize multiplexing of address and data in order to accommodate full 32-bit functionality, along with appropriate control signals, into the 64-pin allotment.

The MVMX32bus Interface on the MVME130 is limited to one master. The interface can be turned off via a control bit to force all accesses to go to the VMEbus, and speed up VMEbus accesses. The MVME130, with one or more MVME204's, creates a memory system with performance similar to that of a VMEmodule with onboard memory, but with virtually unlimited memory size constraints.

MEMORY MAP

The address map, (refer to Table 1) indicates the 32-bit address map for different devices addressed by the MVME130. The 24-bit address map is determined by eliminating the two most significant hex digits from the 32-bit addresses. A control bit on the control register allows the user to switch between 16- and 32-bit data paths, and between 32-/24-bit address modifier codes.

TABLE 1 — Address Map

Device	Physical Address	Comments
VMEbus/MVMX32bus	00000000-FFEFFFFF	32/16-bit port size; R/W.
ROM	FFF00000-FFF8FFFF	16-bit port size; read only. ½ Megabyte
Local Static RAM	FFF20000-FFF2FFFF	16-bit port size; R/W. 64K
Spare	FFF40000-FFF6FFFF	32-bit port size; R/W provided for cache expansion ability.
Timer	FFFBxx00-FFFBxx2F	8-bit port size; R/W.
Status & Control	FFFBxx30-FFFBxx3F	32-bit port size; Status is read only; Control is R/W.
Serial I/O Port	FFFBxx40-FFFBxx5F	8-bit port size; most are R/W.
Reserved	FFFBxx60-FFFBxx6F	Unimplemented.
Spare	FFFBxx70-FFFEFFFF	Unimplemented; Access will cause LBTO (BERR source) cycle termination.
VMEbus Short I/O	FFFF0000-FFFFFFFF	16-bit; R/W; VMEbus Short I/O Address Modifier will be generated.

MVME130
MVME131

PROGRAMMABLE TIMER MODULE

The MVME130 Programmer Timer Module provides the following:

- Three Cascadable, Independent 16-bit Counters
- Interrupt Capability

SERIAL I/O

The MVME130 is equipped with two multiprotocol serial I/O ports with connection via a 50-pin flat ribbon cable connector at the top of the board. Signal levels at this connector correspond to TTL specifications. A transition board/cable/connector (MVME707) is made available to transform the TTL levels to RS-232C and provide a standard DB-25 interface. The ports have the following features:

- Programmable Baud Rates
- Full and Half Duplex Compatibility
- 5- to 8-bits Per Character Plus Parity
- Synchronous or Asynchronous Operation, Including
  - — Byte-oriented protocols (BISYNCH)
  - — Bit-oriented protocols (SDLC)
- Data Rate Capability to 800 Kilobits/Second

STATUS/CONTROL REGISTERS

The MVME130 Status and Control Registers provide local and system wide status information to the on-board MPU. By reading the Status and Control register bits, the MPU can determine VMEbus information, interrupt status, the source of a particular BERR, and which self-test to perform. The MVME130 Status/Control Register bits control the module's hardware by providing configuration and control information to the VMEbus Interrupter, the Interrupt Handler, the VMEbus Arbiter and MVMX32bus. For example, the Multi-Processor Interrupt Request (MPIRQ*) is an input from the VMEbus IRQ1* signal. MPIRQ* enables the user to interrupt several MVME130 modules in a multi-processor system with a single VMEbus interrupt.

The Control Register bits are software alterable. The Status/Control registers are privileged resources and in special cases can be made accessible by the user. The Status Register format is shown in Table 2 and the Control Registers are described in Table 3.

TABLE 2 — Status Register Format

<STAT0>

31 Front Panel Switch Selectable 24

MODE	AMSEL	SC*	GPC	GPB	GPA	GP9	GP8

<STAT1>

23 Front Panel Switch Selectable 16

GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0

|←-------------- Provides VME130 Networking Base Address ------------→|
|←-------------- and useful as general purpose status ---------------→|

<STAT2>

15 Power Up Reset Condition: "1" 08

**	**	ABORT	SYSFAIL*	VBERR*	VXBERR*	MMUBERR*	LBTO*

|←--------- BERR Source Status Register ----------→|

(**denotes: unimplemented — always read as "1").

MODE, AMSEL	<Power Up VMEbus Mode>
SC*	<VMEbus System Controller>
GPC-GP0	<General Purpose User Status Bits>
ABORT	<Abort Pushbutton Status>
SYSFAIL*	<VMEbus System Failure Flag>
VBERR*	<VMEbus BERR Flag>
VXBERR*	<MVMX32bus BERR Flag>
MMUBERR*	<MMU BERR Flag>
LBTO*	<Local Bus Timeout BERR Flag>

TABLE 3 — Control Register Format

<CNT0>

31 — Power Up Reset Condition: "1" — 24

VBV7	VBV6	VBV5	VBV4	VBV3	VBV2	VBV1	VBV0

|←— VMEbus IRQ Vector —→|

|←— Port A on the Z8036 Timer —→|

<CNT1>

31 — Power Up Reset Condition: "1" — 24

MPIRQ*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

|←— Port B on the Z8036 Timer —→|

<CNT2>

31 — Power Up Reset Condition: "1" — 24

VBIMSK7	VBIMSK6	VBIMSK5	VBIMSK4	VBIMSK3	VBIMSK2	VBIMSK1	VBISMSK

|←— which VMEbus IRQ's this Interrupt Handler responds to —→|

<CNT3>

23 — Power Up Reset Condition: "0" — 16

Reserved	ALLIEN	SYSFIEN	Reserved	IL2	IL1	IL0	Reserved

|←— Interrupt Enables —→|←— VME IRQ Request Level, Status —→|

<CNT4>

15 — Power Up Reset Condition; "1" — 08

Reserved	Reserved	Reserved	32/24*	Reserved	Reserved	Reserved	Reserved

<CNT5>

07 — Power Up Reset Condition: "1" — 00

PMEN	VXDIS	VXRR*	VXDEN	UXIRQ	32/24*	32/16*	BDFAIL

VBV7-VBV0	<VMEbus IRQ Vector Number Register>	VXDIS	<MVMX32bus Disable>
MPIRQ*	<Multi-Processor Interrupt Request>	VXRR*	<MVMX32bus Read Only Mode>
VBIMSK7-1	<VMEbus Interrupt Masks>	VXDEN	<MVMX32bus Decode Enable>
VBISMSK	<VMEbus Interrupt Status IRQ Mask>	VXIRQ	<MVMX32bus Interrupt Request>
ALLIEN	<All IRQ Enable>	32/24*	<VMEbus Address Size>
SYSFIEN	<SYSFAIL IRQ Enable>	32/16*	<VMEbus Data Bus Width>
IL2-IL0	<VMEbus IRQ Request Level>	BDFAIL	<Board of System Failure>

MVME130
MVME131

VMEbus INTERFACE

The VMEbus interface provides for VMEbus arbitration; for buffering of data, address, and control signals; for word data manipulation to accommodate MC68020 and VMEbus data handling differences and for Interrupt handling.

The VMEbus arbiter arbitrates up to four levels of bus mastership on a priority basis, utilizes a Pal chip, and incorporates the Release on Request (ROR) option described in the VMEbus specification (MVMEBS/D1).

INTERRUPT HANDLER

The MVME130 allows interrupts to the onboard CPU from up to 20 sources. The interrupt handler preprocesses interrupt sources into three groups of seven interrupts corresponding to the seven possible MC68020 interrupt levels. The groups are labeled Group 1, Group 2, and Group 3. The interrupt service priority is determined by the interrupt level and the group number. Interrupts with different interrupt levels are processed according to the standard interrupt processing discipline. Interrupts within an interrupt level are processed according to the group number.

Group 1 is reserved for VMEbus interrupts. The interrupt handler processes Group 2 and 3 interrupts differently from Group 1 interrupts. If the interrupt being acknowledged is a Group 2 or 3 interrupt, the interrupt handler fetches the appropriate exception vector number from PROM and sends it to the CPU via the local bus. If the interrupt being acknowledged is a Group 1 interrupt, the exception vector number is fetched from the VMEbus where it was placed by the interrupting device.

The Interrupt assignments are described in Table 4.

VMEbus INTERRUPTER

The VMEbus Interrupter can generate any level of VMEbus interrupt under software control. When the VMEbus interrupt is acknowledged, the Interrupter places the appropriate vector from a hardware register on the VMEbus.

TABLE 4 — Interrupt Handler Priority Assignments

IRQ Level	Priority Within a Particular IRQ Level Determines the Service Order		
	(Highest)	(Middle)	(Lowest)
	Group 3	Group 2	Group 1
7	ABORT*	ACFAIL Interrupt ACFIRQ*	IRQ7* (VMEbus)
6	TMRIRQ*	SYSFIRQ*	IRQ6* (VMEbus)
5	SIOIRQ*	VBISIRQ*	IRQ5* (VMEbus)
4	Unassigned	VXIRQ*	IRQ4* (VMEbus)
3	Unassigned	Unassigned	IRQ3* (VMEbus)
2	Unassigned	Unassigned	IRQ2* (VMEbus)
1	N/A	Unassigned	IRQ1* (VMEbus)

Within a Group x, interrupt priority decreases from top to bottom in the table.
Within a particular IRQ level, interrupt priority decreases from left to right.

Group 3 Interrupts

ABORT*	<Abort Pushbutton IRQ>
TMRIRQ*	<Timer IRQ>
SIOIRQ*	<Dual Channel Serial Port IRQ>

Group 2 Interrupts

ACFIRQ*	<VMEbus AC Power Fail Interrupt>
SYSFIRQ*	<VMEbus System Fail Interrupt>
VBISIRQ*	<VMEbus IRQ Request Acknowledge Interrupt>
VXIRQ*	<MVMX32bus Interrupt>

Group 1 Interrupts

IRQ7-1*	<VMEbus Interrupts>

MVME130
MVME131

Mechanical and Environmental Specifications

Characteristics	Specifications
Power Requirements	
MVME130	+5 Vdc, 5 A (typ), 6 A (max)
MVME131	+5 Vdc, 6 A (typ), 7 A (max)
	+12 Vdc, 250 mA (max) −12 Vdc, 250 mA (max)
Clock Signal	12.5 MHz clock frequency
Addressing	
Total system size	4 Gigabytes (32-bit addressing)
ROM/EPROM/RAM	Four 28-pin sockets for 16/32/64Kb devices using +5 Vdc only.
Operating Temperature	0° to 50°C
Storage Temperature	−40° to 85°C
Relative Humidity	5% to 95% (non-condensing)
Physical Dimensions	
Height	6.3 in (16.0 cm)
Width	9.19 in (23.34 cm)
Thickness (MVME130)	.71 in (1.8 cm)
(MVME131)	1.51 in (3.84 cm)

Ordering Information

Part Number	Description
MVME130	VMEmodule 32-bit Monoboard Microcomputer with MC68020 CPU. Includes User's Manual.
MVME131	VMEmodule 32-bit Monoboard Microcomputer with MC68020 CPU and Hardware Memory Management. Includes User's Manual.
MVME130/D	VMEmodule 32-bit Monoboard Microcomputer User's Manual.

Related Product

Part Number	Description
MVME130bug	MVME130bug Debugging Package for VMEmodule 32-bit Monoboard Microcomputer. Includes User's Manual.
MVME204	VMEmodule 1024Kb Dynamic RAM Module with MVMX32bus. Includes User's Manual.
MVME214	VMEmodule Static RAM/ROM Module with MVMX32bus. Includes User's Manual.
MVME707	MVME130 RS-232C Distribution Board with Dual RS-232C Serial I/O Cable Assembly. Includes User's Manual.

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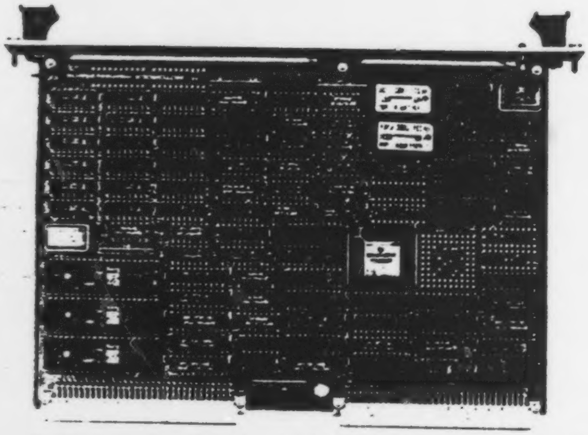
MOTOROLA
MICROSYSTEMS PRODUCTS
TECHNICAL DATA

MVME331
MVME705
MVME706

VMEmodule™ Six-Channel Synchronous/ Asynchronous Communications Controller

- Intelligent Communications Controller (ICC)
- Six RS-232-C or RS-422 Ports (Selection on separate I/O Transition Module)
- Data Transfer Modes:
  - Synchronous 1 Mbit/s, Single Channel
  - Asynchronous 78.6K Baud, Full Duplex, Single Channel
  - 9600 Baud, Full Duplex, 6-Channels, Concurrent
- 128Kb Dynamic RAM (Zero CPU Wait Cycles)
- 10 MHz, MC68010 16-/32-Bit Microprocessor
- Three Z8530 Serial Communications Controllers
- Double High Eurocard Form Factor
- VMEbus Compatible
- Drivers for VERSAdos and SYSTEM V/68 (UNIX) available



The MVME331 Intelligent Communications Controller offers the control and interfaces for six high performance, asynchronous or synchronous serial channels. A microcomputer comprised of an MC68010 Microprocessor, 128Kb of dynamic RAM and a control program in 32Kb of EPROM is used to free a system host of most of the serial communications overhead and achieve high data transfer rates. Each serial port can operate individually at a synchronous data rate of up to one megabit per second or asynchronously at up to 76.8 kilobaud, full duplex. A block diagram of the controller is shown in Figure 1.

The controller is designed for use in VMEbus-based systems requiring high performance. Because it handles all I/O related functions locally without interacting with the host processor, system performance is increased and applications can be more modular and flexible. The controller checks, translates and individually processes received and transmitted characters. It also performs, autonomously, typical peripheral control functions such as echo, software or hardware handshake, insertion and deletion of control characters and line editing. All communication protocol parameters for the six ports are dynamically reconfigurable under software control, providing the maximum in application versatility.

The MVME331 has VMEbus control and status registers which allow a host to send interrupts and commands to the controller and the controller to provide status information to a host.

The ICC firmware contains self-test routines which are executed after system reset. Controller malfunctions are indicated on the front panel by a FAIL LED.

Typical applications for the MVME331 include terminal connection in multiuser systems, connection of asynchronous devices (e.g., printers, PROM programmers), links between computer systems and all types of data acquisition in control environments.

USER INTERFACE

A system host communicates with the MVME331 via an easy-to-use interface that is virtually operating system and serial device independent. Macro commands are sent through a pipeline structure in system memory which is shared by the host and the controller. The commands are retrieved and executed by the controller and a report of execution results is sent to the host through another, similar structure. This software interface complies with the standard Motorola Buffered Pipe Protocol for interprocessor communications.

VMEbus/MVME331/SERIAL DEVICE INTERCONNECTION

VMEbus/MVME331 interconnection is through rows A & C of the rear P2 connector. Signals for all six channels are brought to P2 at TTL levels and require off-board translation of these levels to standard communication values (RS-232-C, RS-422-B or other). Changing to a different protocol thus requires only a new external level shifter — with no change to the MVME331 module or to software. The user may provide this via a bulkhead connector panel or by means of the available transition modules.

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(Replaces NP182)

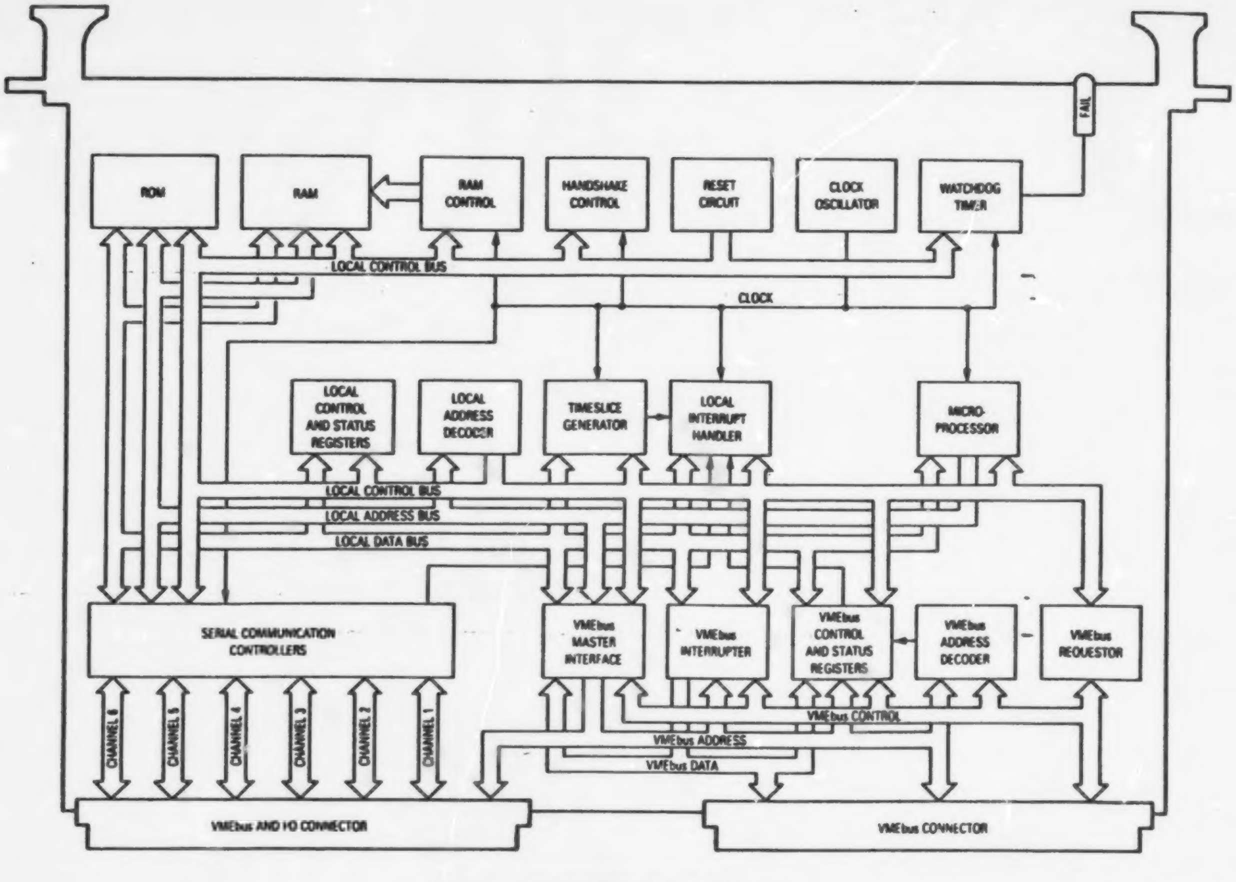

FAIL
ROM
RAM
RAM CONTROL
HANDSHAKE CONTROL
RESET CIRCUIT
CLOCK OSCILLATOR
WATCHDOG TIMER
LOCAL CONTROL BUS
CLOCK
LOCAL CONTROL AND STATUS REGISTERS
LOCAL ADDRESS DECODER
TIMESLICE GENERATOR
LOCAL INTERRUPT HANDLER
MICRO-PROCESSOR
LOCAL CONTROL BUS
LOCAL ADDRESS BUS
LOCAL DATA BUS
SERIAL COMMUNICATION CONTROLLERS
VMEbus MASTER INTERFACE
VMEbus INTERRUPTER
VMEbus CONTROL AND STATUS REGISTERS
VMEbus ADDRESS DECODER
VMEbus REQUESTOR
CHANNEL 6
CHANNEL 5
CHANNEL 4
CHANNEL 3
CHANNEL 2
CHANNEL 1
VMEbus CONTROL
VMEbus ADDRESS
VMEbus DATA
VMEbus AND I/O CONNECTOR
VMEbus CONNECTOR

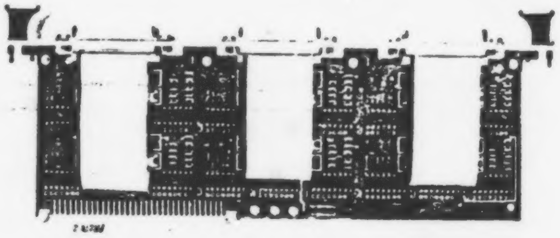
Figure 1. MVME331 Block Diagram

MVME705/706 COMMUNICATIONS TRANSITION MODULES

By means of a separate MVME705 module, any of the six serial channels can be individually configured for RS-232-C or RS-422-B operation. The lower cost MVME706 is pre-configured for the RS-232-C protocol on all six channels. The MVME705 and MVME706 modules provide the receiver and trasmitter circuits for converting the input/output signals of the controller to conform to the requirements of the desired standard. Figure 2 is a block diagram of the MVME705 module.

A transition module is connected to the MVME331's P2 connector via a 64-conductor flat ribbon cable having DIN41612 C64 connectors at each end. Six standard 25-pin subminiature "D" connectors are provided on a transition module's front panel for attaching serial peripheral devices. Each serial port can be configured independently as data circuit terminating equipment (DCE) or as data terminal equipment (DTE) by means of jumpers on the transition module. Tables 1 through 3 provide, for each configuration, the RS-232-C and RS-422-B pin/signal correspondences at the P2 and front panel connectors.

Configuring a channel on the MVME705 for RS-232-C or RS-422-B operation is done by installing in the IC sockets on the module the appropriate transmitter/receiver devices (supplied with the MVME705). The MVME705 package contains all devices required for either operating standard. In addition, the module includes locations in which the user can install capacitors for slew-rate limitation and noise filtering (for RS-232-C) or resistors for balanced line termination (for RS-422-B).



The MVME706 I/O Transition Communications Module is a low-cost pre-configured version of the MVME705 set up for the RS-232-C standard on all channels. The board includes locations for user-supplied slew-rate limiting and noise filtering capacitors.

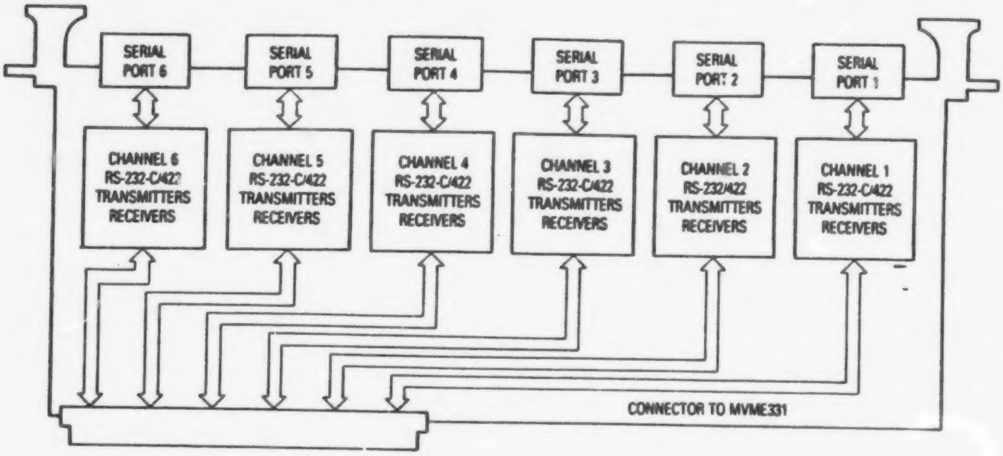

SERIAL PORT 6
SERIAL PORT 5
SERIAL PORT 4
SERIAL PORT 3
SERIAL PORT 2
SERIAL PORT 1
CHANNEL 6 RS-232-C/422 TRANSMITTERS RECEIVERS
CHANNEL 5 RS-232-C/422 TRANSMITTERS RECEIVERS
CHANNEL 4 RS-232-C/422 TRANSMITTERS RECEIVERS
CHANNEL 3 RS-232-C/422 TRANSMITTERS RECEIVERS
CHANNEL 2 RS-232/422 TRANSMITTERS RECEIVERS
CHANNEL 1 RS-232-C/422 TRANSMITTERS RECEIVERS
CONNECTOR TO MVME331

Figure 2. MVME705/706 Functional Block Diagram

Table 1. Serial Port in RS-232-C DTE Configuration

Pin	Signal	Direction	Connected With
2	TXD	output	P2 TXD
3	RXD	input	P2 RXD
4	RTS	output	P2 RTS*
5	CTS	input	P2 CTS*
6	DSR	input	P2 DSR*
7	GND	—	P2 GND
8	DCD	input	P2 DCD* or open
15	TXCI	input	P2 TRXC* or open
17	RXCI	input	P2 RTXC*
20	DTR	output	P2 DTR*
24	TXCO	output	PT TRXC* or open

Table 2. Serial Port in RS-232-C DCE Configuration

Pin	Signal	Direction	Connected With
2	TXD	input	P2 RXD
3	RXD	output	P2 TXD
4	RTS	input	P2 CTS*
5	CTS	output	P2 RTS*
6	DSR	output	P2 DTR*
7	GND	—	P2 GND
8	DCD	output	+ 12 Volts
15	TXCI	output	P2 TRXC* or open
17	RXCI	output	P2 TRXC* or open
20	DTR	input	P2 DSR*
24	TXCO	input	P2 RTXC*

Table 3. Serial Port in RS-422-B Configuration

Pin	Signal	Pin	Signal	Direction	Direction With
2	−TXD	15	+TXD	output	P2 TXD
3	−RXD	16	+RXD	input	P2 RXD
4	−RTS	17	+RTS	output	P2 RTS*
5	−CTS	18	+CTS	input	P2 CTS*
6	−DSR	19	+DSR	input	P2 DSR*
7	GND			—	P2 GND
8	−DCD	21	+DCD	input	P2 DCD* or open
9	−DTR	22	+DTR	output	P2 DTR*
10	−TXCI	23	+TXCI	input	P2 TRXC* or open
11	−TXCO	24	+TXCO	output	P2 TRXC* or open
12	−RXCI	25	+RXCI	input	P2 RTXC*

COMMUNICATIONS CONTROLLER MEMORY

Local memory consists of 32Kb of EPROM and 18 64Kb RAM devices providing a capacity of 128Kb with parity. The EPROMs contain the firmware resident ICC program that is copied to and executed from RAM following power-up reset. The RAM also holds the intermediate I/O data to be processed and transferred. Data is written into and read from RAM without MPU wait states. The generation and checking of byte parity is performed automatically during RAM accesses and a detected parity error causes generation of an autovectored level 7 interrupt to the MPU. Wrong parity can be forced for test purposes by setting the WWP* bit in the module control register. Refresh of the dynamic RAM is automatic with local arbitration logic controlling the access/refresh cycles.

The two provided ROM sockets, one for odd and one for even addresses, can accept a maximum of 128 kilobytes of firmware. Means are included for jumper configuration to accommodate 2764, 27128, 27256 or 27152 type EPROM devices, having access times of 250, 350, or 450 nanoseconds.

VMEbus INTERFACE

For data interchange with a host on the MVMEbus, the controller utilizes an A32:D16 or A24:D16 master interface supported by address decoding logic, address modifier registers and an option Release When Done (RWD) bus requester. System memory accesses are controlled by the option RWD bus requester which can be set by jumper to any one of the four priority levels. Data transfers are supervised by a bus timer with a jumper selectable period. Two access modes are provided: the window addressing mode in which a 4Mb local address map is used as a window to the VMEbus and the alternate space addressing mode in which an address extension register is used to obtain mapping of a contiguous 16Mb address space anywhere within the full 4 gigabyte VMEbus range.

Interrupt requests from the controller to a system host are generated by a VMEbus interrupter having provision for a programmable status/ID byte. When the bus is acquired for MPU accesses, the requester releases on the

VMEbus INTERFACE (Cont.)

next local data transfer. The controller status register contains a bit reflecting the state of the interrupt request output which can be polled by the controller MPU.

An option A16:D16 slave interface accommodates accesses from the VMEbus of the ICC control and status registers. These occupy, in the short I/O address space, a single word which appears redundantly throughout a 128 word segment. By jumper, the segment can be placed on any 256 byte boundary relative to the I/O space base address. A write operation accesses the VME control register. A read operation accesses the VME status register.

Short supervisory and non-privileged access of the short I/O space is provided by a bipolar PROM which decodes address modifier codes $29 and $2D. The PROM may be reprogrammed if use of other codes is desired.

Tables 4 and 5 identify, respectively, the connectors P1 and P2 pin/VMEbus signal assigments.

Table 4. Connector P1 VMEbus Signal Locations

Pin No.	Row A Signals	Row B Signals	Row C Signals	Pin No.
1	D00	BBSY*	D08	1
2	D01	(BCLR*)	D09	2
3	D02	(ACFAIL*)	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	(SYSCLK)	BG3IN*	SYSFAIL*	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	BR0*	SYSRESET*	12
13	DSO*	BR*	LWORD*	13
14	WRITE*	BR2*	AM5	14
15	GND	BR3*	A23	15
16	DTACK*	AM0	A22	16
17	GND	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	(SERCLK)	A17	21
22	IACKOUT*	(SERDAT)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A4	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	– 12 V	(5 V STBY)	+ 12 V	31
32	+5 V	+5 V	+5 V	32

Note: Signals in parentheses are not used by the MVME331.

Table 5. Connector P2 Signal Locations

Pin No.	Row A Signals	Row B Signals	Row C Signals	Pin No.
1	+5 V	+5 V	+5 V	1
2	– 12 V	GND	+ 12 V	2
3	TRXC6*	(RESERVED)	GND	3
4	DTR6*	A24	DCD6*	4
5	CTS6*	A25	DSR6*	5
6	RXD6	A26	RTS6*	6
7	TXD6	A27	RTXC6*	7
8	TRXC5*	A28	GND	8
9	DTR5*	A29	DCD5*	9
10	CTS5*	A30	DSR5*	10
11	TXD5	A31	RTS5*	11
12	TXD5	GND	RTXC5*	12
13	TRXC4*	+5 V	GND	13
14	DTR4*	(D16)	DCD4*	14
15	CTS4*	(D17)	DSR4*	15
16	RXD4	(D18)	RTS4*	16
17	TXD4	(D19)	RTXC4*	17
18	TRXC3*	(D20)	GND	18
19	DTR3*	(D21)	DCD3*	19
20	CTS3*	(D22)	DSR3*	20
21	RXD3	(D23)	RTS3*	21
22	TXD3	GND	RTXC3*	22
23	TRXC2*	(D24)	GND	23
24	DTR2*	(D25)	DCD2*	24
25	CTS2*	(D26)	DSR2*	25
26	RXD2	(D27)	RTS2*	26
27	TXD2	(D28)	RTXC2*	27
28	TRXC1*	(D29)	GND	28
29	DTR1*	(D30)	DCD1*	29
30	CTS1*	(D31)	DSR1*	30
31	RXD1	GND	RTS1*	31
32	TXD1	+5 V	RTXC1*	32

Note: Signals in parentheses are not used by the MVME331. I/O signals are at TTL levels.

PERIPHERAL INTERFACE

Asynchronous and synchronous transfer of data through the serial channels is effected using three Z8530 Serial Communication Controller (SCC) devices. Each offers two independent, full duplex serial channels, is capable of transferring data at rates up to 1 Mbit per second over a single channel and provides the hardware support for the software control of communication modes and protocols. Control provided by the SCC devices allows the independent selection of an encoding mode and the programming of parameters for synchronous or asynchronous operation of any serial channel.

Signals at the TTL level are provided at the VMEbus P2 connector and, by means of a separate communications transition module which also provides the serial port connectors, are translated to the levels and connections required by the RS-232-C or RS-422-B communications standards. The communications signal assignments to pins in connector P2 are identified in Table 5.

The SCC devices are clocked at 4.9152 MHz. By division of this frequency, all baud rates for serial data transfer are generated.

ASYNCHRONOUS OPERATION

When asynchronous data transfer is required, the following parameters can be programmed:

- baud rate from 50 to 76800
- odd, even or no parity
- 1, 1.5 or 2 stop bits
- character length of from 5 to 8 bits
- NRZ, NRZI or FM data encoding

SYNCHRONOUS OPERATION

Transfer of both bit and byte data is supported and the SCC devices can be programmed for a number of different synchronization modes.

Both monosync and bisync modes with or without CRC checking can be used for byte data transfer.

The SDLC or the HDLC protocol with automatic CRC generation and checking can be used for the transfer of bit data. An underrun causes generation of an interrupt to the MPU.

For the synchronous transfer of byte or bit data, odd, even or no parity may be programmed and NRZ, NRZI or FM coding may be selected.

COMMUNICATIONS CONTROLLER TIMER/COUNTERS

The MVME331 Communications Controller contains three timer/counters used for periodic interrupt generation, for the monitoring of module malfunctions and for supervising accesses of the module's data transfer bus and accesses of the VMEbus.

TIMER-SLICE COUNTER

To facilitate the generation of firmware which takes advantage of the powerful data transfer capabilities offered by the serial communications controllers, a programmable timer is included which is used for the generation of periodic interrupts to the module MPU as a basis for the time-slice driven resident executive.

A value is loaded into an 8-bit register, counted down to zero and the resulting output used to generate an autovectored level 2 interrupt request. The interrupt request is latched and reset when acknowledged by the MPU.

Clocked at 78.125 kHz, the counter offers time periods ranging between 3.25 and 12.8 microseconds. The counter can also be disabled and restarted by program instructions.

WATCHDOG TIMER

To provide user software a means of indicating fatal MVME331 malfunctions, a timer with a period of 100 milliseconds is provided on the controller module. On timing out, this timer sets the fail bit in the status register, lights the fail LED on the module front panel and may be jumpered to cause assertion of the VMEbus SYSFAIL* line. User software prevents timeout of the counter by simply accessing the watchdog timer reset location.

DATA TRANSFER BUS TIMER

For supervision of all MPU data transfer cycles on both the local bus and the VMEbus, the MVME331 module includes a timer which generates a local bus error signal if an accessed device fails to respond with a data transfer acknowledge signal before the counter times out. The timeout period is fixed at 25 microseconds for all accesses to local devices. For VMEbus accesses, a timeout period of 25, 50 or 100 microseconds is jumper selectable. The selected period should exceed the greatest time expected to elapse between the assertion of a bus request and the reception of a bus grant in the actual system configuration.

HOST/CONTROLLER COMMUNICATIONS

In order for two intelligent devices to communicate with each other, a channel must exist. In a bus-based system, two kinds of channels are commonly used: physical and logical.

Operation of a physical channel depends on memory which can be shared by the two devices. Often this is dual-ported RAM located on a peripheral device controller in which the host CPU writes commands for execution and in which the controller reports the results of executing the commands. Coherent use of the dual-ported memory as a communications channel generally requires a buffer with its own semaphore register for passing commands and a separate buffer/semaphore register for reporting status.

The other type of communications channel — logical — depends on the sharing of a region of system RAM for the exchange of messages. This concept offers the significant advantage of not being constrained by the size of dual-ported RAM on board an intelligent module. Motorola's Buffered Pipe Protocol facilitates the implementation of logical communications channels.

THE BUFFERED PIPE PROTOCOL

Motorola's Buffered Pipe Protocol defines a communications channel which uses two queues of the FIFO type in system RAM for the exchange of commands and status reports between a system host and an intelligent peripheral device. The buffered pipe implementation exhibits the following features:

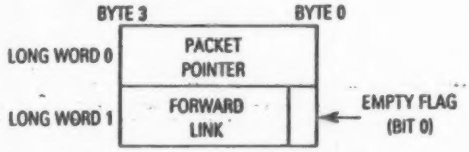
- Broadly Usable — Virtually Operating System and Board Independent
- Supports both Interrupt-driven and Polled Modes of Operation
- Minimizes Hardware — Imposes only Ability to Access System RAM and Interrupt VMEbus Devices
- Non-busy Interface — Always Accessible
- Infinite Queue — Virtually no Message Quantity Restriction
- No Worst Case Handling — Send/Receive Using One Small Set of Instructions
- Simple — Uses a Few Simple Procedure Calls and One, Simple Data Structure
- Symmetrical — Uses Same Mechanism for Virtually all Communication Between Two Processors
- Tolerant — Does Not Restrict Message Content in any Way
- Flexible — Processors Receive Messages in Sent Order but are not Required to Process them in Sent Order

PROTOCOL ELEMENTS

There are four principal elements utilized in the buffered pipe protocol, as shown in the diagrams: a put pointer associated with a sender, a get pointer associated with a receiver, the Buffered Pipe Envelope (BPE) and the command/status/data packet. An envelope is simply two pointers: one to the next envelope and one to the packet associated with the current envelope. The packet is a fixed length data structure residing anywhere in system memory and containing commands, status reports or other parameters. To ensure that a new envelope can be queued by a processor at any time, the protocol prescribes that the last envelope have no associated packet, that its forward link act also as the empty envelope flag by pointing to an odd address (rather than the even address at which a full envelope is required to reside) and that no receiver dequeue this last envelope from the pipe.

CHANNEL INITIALIZATION

Two buffered pipes are used for a MVME331 communication channel: one in which a system driver sends commands and configuration information to a device controller and one in which the controller sends status reports to the driver. Since the communication channel is interrupt driven, each interrupts the other following the queuing or dequeuing of an envelope. It is incument on the driver to initialize the channel and controller by: creating from system memory a pool of envelopes and a pool of packets, initializing a command pipe and a status pipe by placing an empty envelope in each, initializing the command get and status get pointers and passing these to the device controller using the Get Pointers command. This is a command supported by the controller firmware which uses interrupt handshaking for passing a sequence of bytes via the controller's control register. The number of packets required and processing overhead are both minimized by requiring the controller to return status in the same packet in which a command is received.



Buffered Pipe Envelope (BPE)

MVME331/DRIVER COMMUNICATIONS

Communications between a host driver and devices connected to MVME331 serial ports are supported by firmware in 32Kb of ROM onboard the controller module. This firmware observes the Motorola standard buffered pipe protocol for host/intelligent device communications and facilitates initialization and full runtime control of serial device communication modes, codes and protocols. The versatile control and character processing provided by the MVME331 firmware and hardware relieves a system host of much of the overhead imposed when six asynchronous communication channels are operated concurrently.

The MVME331 firmware architecture utilizes a time slice driven, multitasking executive to control read and write channels each of which has a buffer, a dynamic queue and three actions tables. The buffers reduce loading of the VMEbus by allowing transmission of 16 byte blocks for a single bus arbitration cycle and the 256 byte queues aid Xon/Xoff control of the rate of data flow.

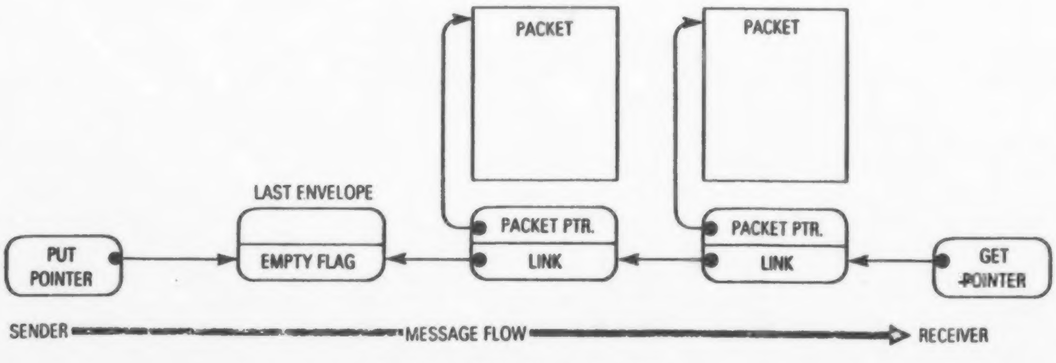
Overall control of the data flow is implemented by using tables to perform character translation so that different codes can be accommodated, to provide control character services, to handle escape key sequences, and to provide editing functions like echo/delete character or cancel line. The tables provide great versatility since to the standard functions provided by the firmware, a user can add control routines to each table to comply with the specific requirements of nearly any application.

READ CHARACTER FLOW

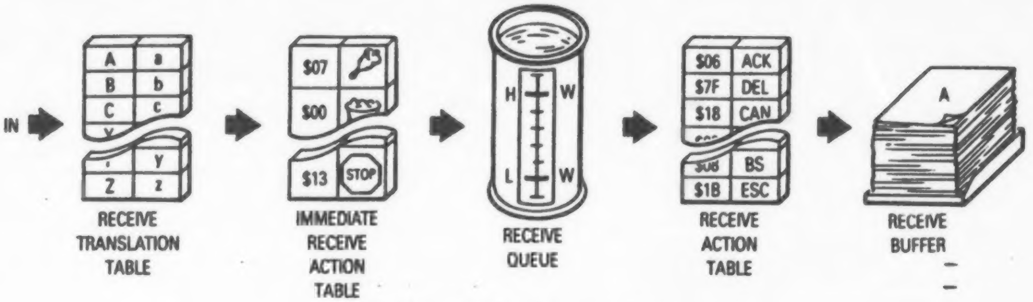
As the diagram shows, the read character flow is: serial port --> Receive Translation Table --> Immediate Receive Action Table --> Receive Queue --> Receive Action Table --> Receive Buffer --> VMEbus.

From a serial device and following any required code translation called for in the Receive Translation Table, characters are sent to the Immediate Receive Action Table where they're screened against values in the Immediate Receive Action Table. Ordinary data characters are passed to the Receive Queue but codes requiring an immediate action such as the use of Xoff to stop transmission on that channel are detected and acted on. The table is also used for other functions such as stripping fill characters so that they do not occupy queue space.

On leaving the Receive Queue, a character is screened against values in the Receive Action Table where other



Buffered Pipe Message Flow



MVME331 Read Character Flow

requirements are detected and acted on. Primarily, these include the support of editing functions such as deleting characters and canceling lines as well as the accommodation of any variance in escape sequences between different kinds of terminals. Before being placed on the VMEbus, characters are sent to the Receive Buffer which facilitates transmission of small bursts rather than single characters.

As the diagram shows, the write character flow is: VMEbus --> Transmit Buffer --> Write Action Table --> Transmit Action Table --> Transmit Queue --> Transmit Translation Table --> Serial Port.

WRITE CHARACTER FLOW

From the VMEbus, bursts of characters are stored in the Transmit Buffer, from which they march single file into the Write Action Table where they are screened. Ordinary data characters are sent directly to the Transmit Queue but a few non-data characters initiate an immediate action such as the sending of a line termination string after a carriage return character. All other non-data characters are sent to the Transmit Action Table where their corresponding editing functions and transmission requirements are identified and performed. From the Transmit Queue, data characters are moved to the Transmit Translation Table for code translation, if required, before they are transmitted through a serial port.

The two communication paths do not operate in total independence particularly when the mode is full duplex. The Receive Action Table, for instance, communicates directly with the Transmit Action Table on receiving a line termination code.

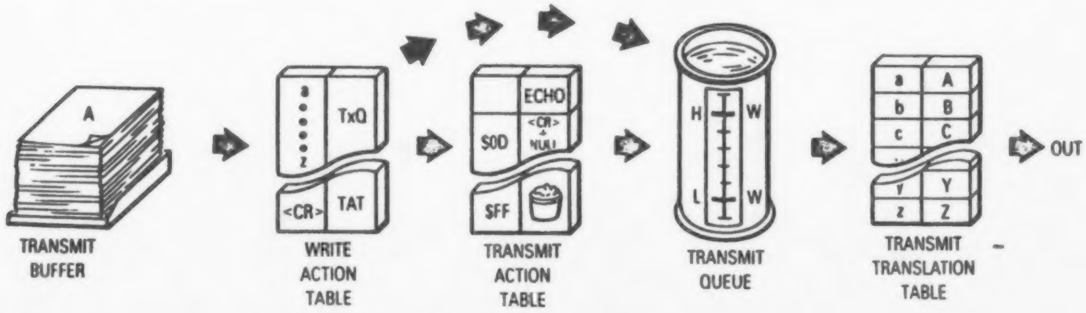
Codes for the standard commands supported by the MVME331 Intelligent Communications Controller (ICC) firmware are shown in Table 6. Codes for standard status messages used for reporting execution status for the commands of Table 6 are shown in Table 7. For a particular application, the user can add commands and status messages, as required.

Table 6. MVME331 Firmware Command List

Code	Command	Code	Command
$01	Read	$0C	Request Port Status
$02	Write	$0D	Request Table Status
$03	Abort	$0E	Reset Port
$04	Solicit Event	$0F	Send Break
$05	Configure ICC	$10	Flush Receive Queue
$06	Configure Port	$11	Flush Transmit Queue
$07	Configure Table	$12	Boot
$0B	Request ICC Status	$13	Go

Table 7. MVME331 Status Messages

Code	Terminating Condition	Code	Terminating Condition
$00	Normal command termination	$0A	Invalid type of parity
$01	End of system memory block	$0B	Invalid handshake selection
$02	Read timeout	$0C	Rx queue overrun
$03	Write timeout	$0D	Invalid delete character string length
$04	Command aborted	$10	Invalid start address
$05	Insufficient local memory	$14	Least number of characters received
$06	Invalid item number	$81	Parity error
$07	Invalid baud rate	$82	Overrun error
$08	Invalid number of bits per character	$83	Overrun and parity error
$09	Invalid number of stop bits	$84	Framing error
		$85	Overrun and framing error



MVME331 Write Character Flow

MVME331 SPECIFICATIONS

Characteristics	Specifications
General	The MVME331 Intelligent Communications Controller is a VMEmodule for interfacing six asynchronous serial communication channels to a VME system.
Performance	The MVME331 can simultaneously control six channels at 9600 baud full duplex with individual character translation and control code processing for each channel.
Local Microcomputer	The local microcomputer consists of a 10 MHz MC68010 microprocessor, 32Kb ROM, 128Kb RAM, interrupt handling logic, and various timers.
VMEbus Interface	The control and status registers on the ICC are accessed from the VMEbus through an option A16:D16 slave interface. The ICC accesses system memory through an option A32:D16 or A24:D16 master interface and supervises data transfers with a bus timer of variable length. The option RWD bus requester can be selected to operate on any one of the priority levels. The priority level and the status/ID byte of the interrupter are software programmable.
Peripheral Interface	Serial link control and data transfer are performed by three Z8530 Serial Communications Controller devices. Baud rates (50 to 76800), data characteristics (number of data bits and stop bits, even or odd parity) and control signal functions (DTR, DSR, RTS, CTS, DCD) are independently selectable for each of the six channels.
Operating System Interface	The transfer of commands, status messages and data packets is performed through a pipeline in VME system memory. This transfer follows the Motorola standard Buffered Pipe Protocol for processor to processor communication. Drivers are available for VERSAdos and SYSTEM V/68.
ICC Commands	The ICC commands include: — ICC configuration — Port configuration — Data read and write operations — Break transmission — Software download and start — Reset and abort functions
ICC Status Messages	The ICC status messages include: — Normal command completion — ICC and port status — Parity and framing errors — Break detection — Data overrun and buffer overflow — Read and write time-out — Invalid commands and parameters
Indicator	FAIL LED on the front panel
Power Requirements	+5 Vdc (±5%), 3.8 A typ, 4.4 A max
Operating Temperature	0° to 55°C Inlet air, forced air cooling
Storage Temperature	−40° to 100°C
Relative Humidity	0% to 90% (non-condensing)
Physical Dimensions Height Depth Front Panel	Double High VME board with front panel 9.2 in. (233 mm) 6.3 in. (160 mm) 10.3 in. (262 mm) 0.8 in. (20 mm)

MVME705 SPECIFICATIONS

Charateristics	Specifications
General	The MVME705 module provides transmitter and receiver circuits for the MVME331 Intelligent Communications Controller module. Both modules are interconnected with a 64-conductor flat-ribbon cable. The serial port signals are available at 25-pin connectors on the front panel.
Serial Port Characteristics	Each channel can be configured for the RS-232-C or RS-422-B EIA standard. The front panel connectors can be configured as data circuit terminating equipment or as data terminal equipment.
Supported Signals	The MVME705 supports the following signals: TXD — Transmitted Data RXD — Received Data RTS — Request To Send CTS — Clear To Send DSR — Data Set Ready DTR — Data Terminal Ready DCD — Data Carrier Detect TRXC — Transmitter-Receiver Clock RTXC — Receiver-Transmitter Clock
Additional User Options	The user can install capacitors for slew-rate limitation and noise filtering (for RS-232-C) and resistors for balanced line termination (for RS-422) on free locations on the board.
Physical Dimensions	Double-high/reduced depth VMEboard
Height	9.2 in. (233 mm)
Depth	3.5 in. (80 mm)
Front Panel	10.3 in. (262 mm) x 1.57 in. (40 mm)
Connectors	One 64-pin DIN41612 connector to the MVME331. Six 25-pin Sub-D serial port connectors.
Power Requirements	+5 Vdc, 1.5 A (max) ±12 Vdc, 150 mA (max)
Operating Temperature	0°C to 55°C Inlet air, forced air cooling
Storage Temperature	−40° to 100°C
Relative Humidity	0% to 90% (non-condensing)

ORDERING INFORMATION

Part Number	Description
MVME331	Six-Channel Intelligent Communication Controller. Includes User's Manual.
MVME705	I/O Transition Communications Module with RS-232 or RS-422 interface. Includes User's Manual.
MVME706	I/O Transition Communications Module with RS-232 interface only. Includes User's Manual.
M68V1XS331DRV	VERSAdos Driver on 5-1/4" diskette (source)
M68N1XB331DRV	SYSTEM V/68 Driver on 5-1/4" diskette (binary)
M68N1XS331DRV	SYSTEM V/68 driver on 5-1/4" diskette (source)

RELATED DOCUMENTATION

HB212/D	VMEbus Specification Manual.

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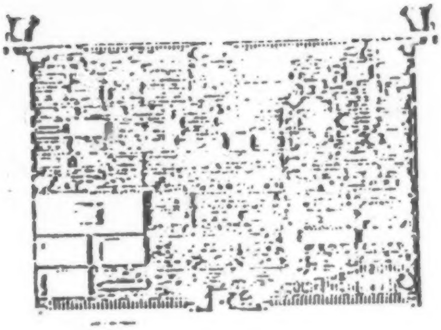
ADVANCE INFORMATION

MVME320

VMEmodule Winchester/Floppy Disk Controller



- Controls Mixed 5¼" and 8" Drives Up to Two Winchester Hard and Two Floppy Disk Drives or up to Four Floppy Disk Drives
- Provides High Performance DMA Data Channels
- Programmable Data Transfer Mode Two Byte or 200 Microsecond Block
- Supports Serial Data Rates up to 5 Megabits Per Second
- Uses Standard IBM Formats and FM and MFM Recording
- User-Programmed Hard Disk Format
- Supports Soft Sectored Drives
- Multiple-sector read/write
- Implied Seek
- Bit Serial 16-Bit CRC/32-Bit ECC Generator
- Automatic Bad Sector Handling
- Single Phase Write and Read Clocks
- Data Transfer — 16-Bit DMA 8-Bit Register
- Self Diagnostics
- VMEbus Requester and Interrupter
- 0°C to +50°C Operating Temperature Range
- VMEbus Compatible

The Disk Controller is a double high Eurocard module for adding mass storage capacity to a VMEbus system. It provides high performance DMA data channels between system memory and Winchester hard disk drives and/or floppy disk drives. The module is used in applications having intensive real-time disk I/O or multiprocessing structures to reduce VMEbus traffic and increase system throughput. Figure 1 is a functional block diagram of the controller module.

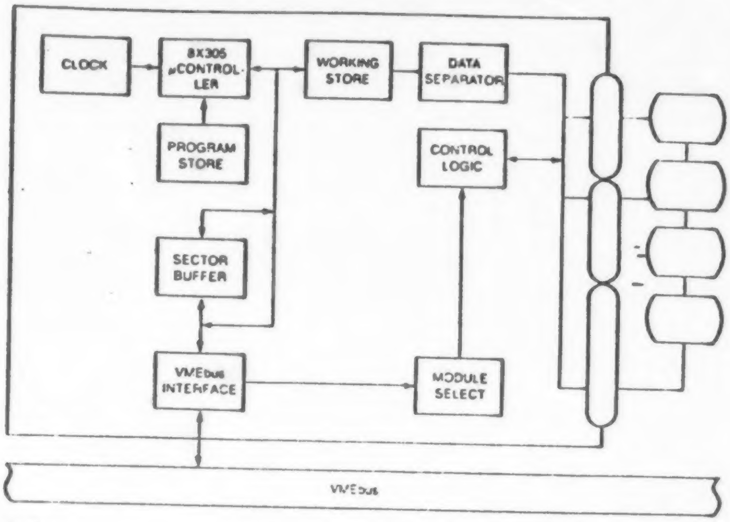
Host/MVME320 Communications

An intelligent module, the disk controller offers the user a high level, easy to program interface. Microinstructions in a 4K × 24 ROM are executed on a Signetics 8X305 Microcontroller at a 200 ns per instruction rate to provide the macro I/O activities requested by the user program.

To a driver running under the host operating system, the controller appears as seven 8-bit control registers at the base address of the module, one block of global memory for each disk drive and a table in global memory of pointers to the starting address of each block. General control of module operations is obtained using the seven registers to pass initialization, vector number, first pointer address and command initiation information to the controller and to obtain interrupt source and drive status information from the module.

The other host/module communications avenue is the event control areas (ECA) which are memory blocks used to convey drive control parameters and command execution parameters from host to module and the status of executed commands from module to host. An ECA comprising static and dynamic fields is created by the host when requesting execution of a command. Static fields remain unchanged. Dynamic fields are used during execution and updated at completion by the controller.

FIGURE 1 — Disk Controller Block Diagram



Disk Drive Interface

The disk interface consists of two sections:

- Input and output ports that sense and generate slow changing or static control signals
- Serial data I/O and high speed disk control circuitry
- Because both sections are serviced by the fast 8X305 microcontroller, the module is able to control a variety of disk types and media formats

Up to four disk drives can be interfaced to the module. Of these two can be Winchester 5¼" or 8" hard disk and two can be 5¼" or 8" floppy disk. If all are floppy, four can be used. Mixed single and double sided floppy disk drives of single or double density are supported.

All head positioning (up to 1024 cylinders/drive) and head selection (up to 16 heads/drive) is automatically provided by the controller for host requested I/O.

Table 1 is a partial list of disk drives which can be used with the controller module.

Data Transfer Modes

On command request, the host specifies the desired transfer mode using the DMA Type field in the ECA. Two DMA data transfer modes are available: two byte and 200 μs block. In the two byte mode, the VMEbus is requested, two consecutive bytes are transferred and the bus released. In the 200 μs mode, the bus is requested, data is transferred for 200 μs and the bus released.

Data Interface

For a requested read or write operation, data is automatically transferred between any of the four disk drives and system memory which can be located anywhere in the VMEbus 16 megabyte address space.

Floppy disk data transfer is done using two byte buffering. For hard disks, a 1024 byte local buffer is used. Automatic head switching and cylinder positioning is performed for operations requiring multiple sector read or write.

Module design uses a multiplexer to transfer disk data to a phase locked loop data separator before sending it to serializer/deserializer (SERDES) circuitry. This section converts serial disk data to parallel for bus transfer and parallel bus data to serial for transfer to disk. The SERDES section also generates and checks CRC code and has a watchdog circuit that monitors the various disk operations for timely completion. The number of retries of an operation that the module will attempt is programmable.

Error Detection And Correction

To insure data integrity, the module provides two software selectable modes of data validation: 16-bit cyclic redundancy check (CRC) or 32-bit error checking and correction (ECC). The ECC algorithm used can correct errors separated in data by as many as 11 bits.

TABLE 1 — MVME320—Compatible Disk Drives

Hard Disk Drives	
8"	5¼"
Shugart SA1000 Series Quantum Q2000 Data Peripherals	Seagate ST506, ST512, ST406, ST412 Shugart SA600 RMS500, RMS506, RMS512 Tandon International Memories Inc.
Floppy Disk Drives	
8"	5¼"
Shugart SA800, SA801, SA810, SA850	Amlyn 5850 Shugart SA400, SA410, SA450

TABLE 2 — Disk Controller Command Set

Command	Description
CALB	Recalibrate (reposition head) to track zero.
RETD	From first sector encountered, return flag, ID, CRC and read-generated remainder.
REMS	Using implied seek, read multiple sectors.
WRMS	Using implied seek, write multiple sectors.
FORM	Using implied seek, format tracks.
WRDD	Write using deleted data address mark flag
VER	Using implied seek, verify data (no transfer).
TSR	Transparent sector read (ignore CRC/ECC errors).
CORR	Using ECC remainder, correct data in memory.

Mechanical And Environmental Specifications

Characteristics	Specifications
Configuration	DTB Master: A24, D16 DTB Slave: A24, D8
Form Factor	Double High Eurocard
Power Requirements	+5.0 Vdc at 2.6 A (typ) +12 Vdc at 20 mA (typ) −12 Vdc at 20 mA (typ)
Environment Limits	
Operating Temperature	0°C to +50°C
Storage Temperature	−55°C to +85°C
Humidity	8% to 80% (non-condensing)
Physical Characteristics	
PC Board Height	9.2 in. (234 mm)
PC Board Depth	6.3 in. (160 mm)

Command Set

The controller module offers the set of nine high level commands listed in Table 2.

Control Program PROM Size Selection

The module has a header to allow selection of a 2K × 8 or 4K × 8 size for the three PROMs in which the control program is stored. This header is wired for the 4K × 8 PROMs shipped with the module.

Base Address Selection

The module has a header for jumper selection of a base address which can be set on any 1K byte boundary throughout the 16 megabyte VMEbus address space.

Address Modifier Code Selection

The module has a header for selection of response to address modifier codes for user (hex 29) and supervisor (hex 2D) or for response to the supervisor code only. As shipped, the module responds to both codes.

VMEbus Interrupter

The module has circuitry for generating an interrupt on six of the seven VMEbus interrupt priority and interrupt acknowledge levels: 1 through 6. Selection of an interrupt and an acknowledge level is accomplished by jumper in the corresponding headers. As shipped, both levels are set at 3.

VMEbus Requester

The module has the logic required to request mastership of the data transfer bus (DTB) on any one of the four bus request and four bus release levels and for operation in the release-when-done mode. The module has two headers for jumper selection of one of the four bus request levels and one of the four bus grant levels. As shipped, both are set for level 3.

Software Driver

A driver for the disk controller module is incorporated in the 4.4 release of the VERSAdos Operating System and is also available as a separate product. The driver supports interface with the drives listed in Table 1. For users desiring to write their own driver, a manual, Guide To Writing Device Drivers for VERSAdos, M68DRVGD/D1, detailing how to write a driver that runs under the M68000 Real-Time Multitasking kernel or under VERSAdos is available.

Disk Controller Usage

The Disk Controller can be used as a slave in a VMEbus system in which any of the monoboard microcomputers listed in Table 3 operates as bus master. Table 3 lists the disk controllers for which bootstrap, load and dump capabilities are provided by the debugger supplied with the corresponding microcomputer.

TABLE 3 — Boot/Load/Dump Support

Microcomputer	Debugger Supported Disk Controllers
MVME101	MVME315
MVME110-1	MVME315, MVME320, M68RWIN1, MVME420/SA1403D
MVME115M	MVME320, M68RWIN1*

*Using the MVME316 VMEbus-To-I/O Channel Interface

Ordering Information

Part Number	Description
MVME320	VMEmodule Winchester/Floppy Disk Controller
MVME320/D1	VMEmodule Winchester/Floppy Disk Controller User's Manual

Related Documentation

Part Number	Description
MVMEBS/D1	VMEbus Specification Manual
M68DRVGD/D1	Guide to Writing Device Drivers For VERSAdos

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SYSTEM PRODUCT
TECHNICAL DATA

MVME204

Advance Information

VMEmodule

1024Kb Dynamic RAM w/MVMX32bus*

- Supports VMEbus/MVMX32bus
- Dual Ported — 32-bit address and data VMEbus and multiplexed 32-bit address/data MVMX32bus interface
- Interleaving — Two-way interleaving on VMEbus or MVMX32bus
- Configurable Array — Dynamically alterable to be partially or fully private to the MVMX32bus port. Selectable in 1/4 population increments
- Byte Parity Generation and Error Checking Circuitry
- Longword (32-bit), Word (16-bit), or Byte (8-bit) Data Transfers
- VMEbus Addressing — Automatic selection of 24- or 32-bit addressing on VMEbus interface, 32-bit addressing on MVMX32bus
- Memory Base Address Settable onboard size boundaries throughout VMEbus and MVMX32bus Address Space
- Transparent Refresh Support

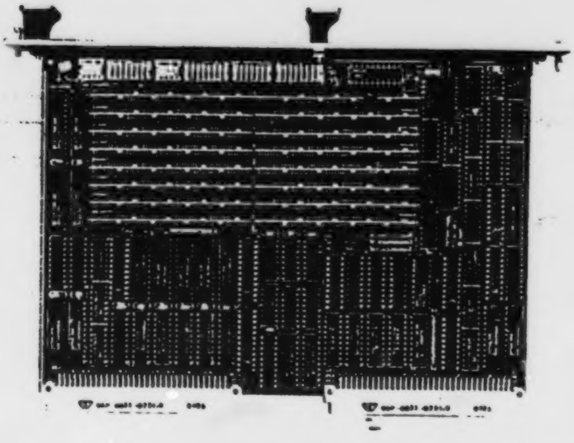
FUNCTIONAL DESCRIPTION

The MVME204 is a dual ported 1024Kb dynamic RAM module with parity for use with VMEbus and MVMX32bus. The MVME204/MVMX32bus interface is tailored to the MC68020 microprocessor and is specifically designed to enhance the performance of the MVME130 VMEmodule 32-bit Monoboard Microcomputer. The MVMX32bus interface, since it is a high-speed dedicated memory bus, allows concurrent DMA transfers on VMEbus with MVMX32bus transfers between the MVME130 and MVME204.

The MVME204 attains its capacity and performance using high density 64K×1-bit dynamic RAM devices. The MVME204 has parity generation and detection circuitry which, together with accessible control and status registers, can be used for error detection and memory diagnostics.

Because of its VMEbus interface, the MVME204 can be used in systems using this interconnect structure. Care must be used with existing VMEmodule-based systems, since MVMX32bus and the extended 32-bit data and address use P2 of the VMEbus connector. The pins on connector P2 of the existing VMEbus system are commonly used as I/O pins.

Figure 1 is a functional block diagram of the MVME204.



VMEbus ADDRESS MAPPING

The MVME204 has two switches (12 bits) used to set module memory to begin on any 1024Kb boundary.

The ending address of module memory is the sum of the starting address and the board population.

The MVME204 utilizes one byte within VMEbus I/O Space as a location for the control/status register. Selection of the control/status register location within the VMEbus I/O address range is switch selectable.

VMEbus ADDRESS MODIFIER CODE RESPONSE

VMEbus address modifier line decoding on the MVME204 provides response to both standard and extended, supervisory and non-privileged program and data accesses. The short supervisory I/O access code (15 hex) must be placed on the address modifier lines to access the control/status register.

A programmable array logic device (PAL) is used for address modifier line decoding. This PAL is socketed to facilitate application of the MVME204 in systems having special requirements.

MVMX32bus ADDRESS MAPPING

The MVME204 has two switches (12 bits) used to set module memory to begin on any 1024Kb boundary. The ending address of module memory is the sum of the starting address and the board population.

Global/Private memory mapping is dynamically alterable via the status/control register. One bit enables MVMX32bus private mode. Alternately, two bits determine the size of the private memory in 256Kb segments. The private memory is

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*MVMX32bus is a Motorola Proprietary Expansion bus for use with VMEbus.
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allocated from the upper to lower segments on the MVME204. The system integrator, at the time private memory is allocated, must be cognizant of any holes that may be introduced into the memory map due to the allocation of private memory.

STATUS/CONTROL REGISTER

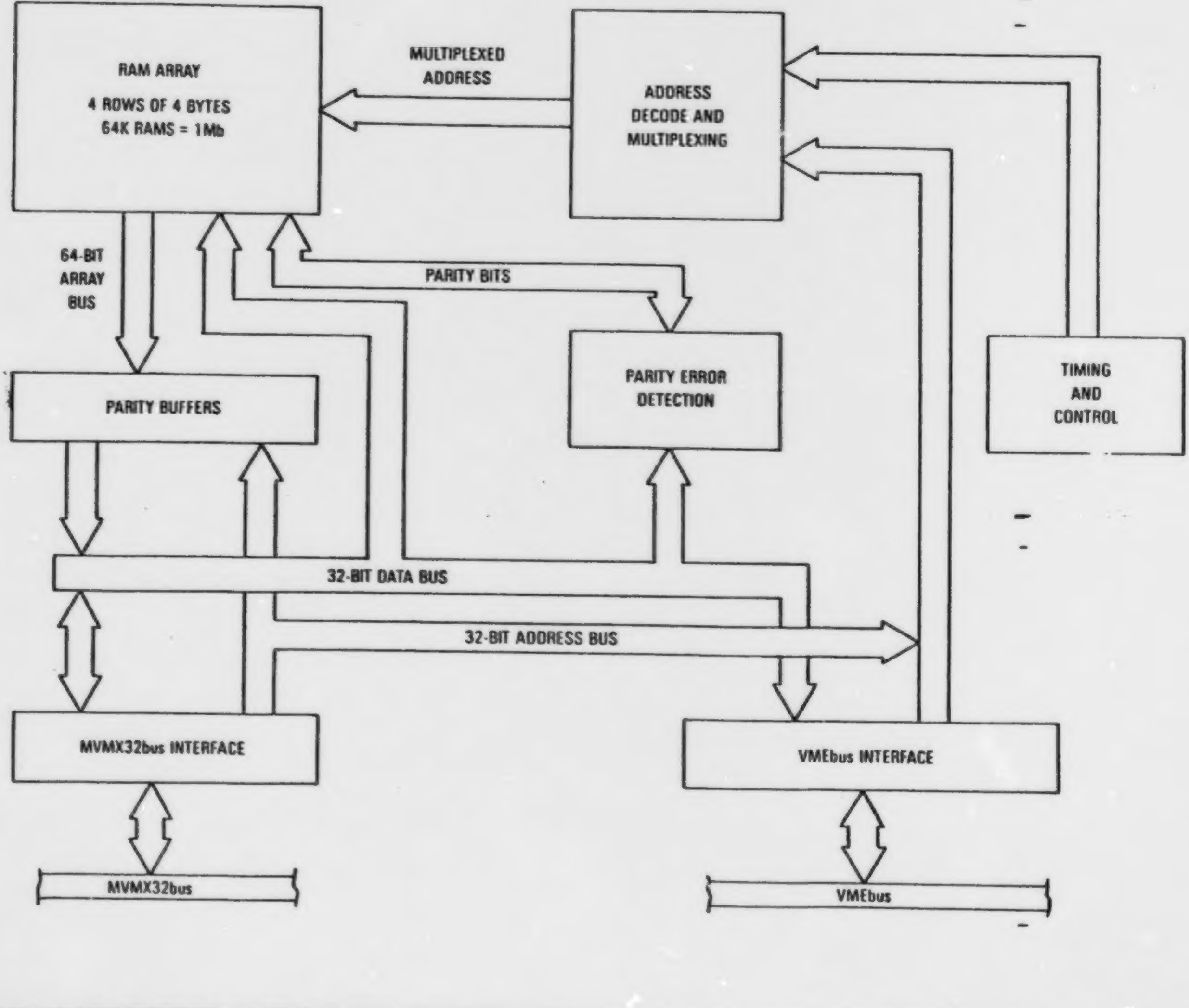
The MVME204 status/control block provides VMEbus accessible registers for MVME204 control and status. The control register is writable and readable from the VMEbus. The only status is parity error Bit 7 of the control register. The control and status registers are reset at power up. The Parity Error Status bit is settable or resettable by writing a zero to Bit 7 of the control register. The control and status registers are defined below.

PARITY FUNCTIONS

In normal operation, the MVME204 generates and writes an odd parity bit with each byte stored in its memory. When a byte is read, odd parity is again generated and compared with the stored parity bit. Bit 7 in the control/status register is set wherever an error is detected. On detection of an error, when EPER is set, the VMEbus BERR* or MVMX32bus MERR* signal line is driven low and Bit 7 in the control/status register is set.

To facilitate the testing of memory, the control/status register has two bits for software control of (1) enable parity error reporting and (2) wrong parity generation. Bit 1 may be set to enable the writing of the wrong parity value into a parity bit. Bit 0 enables bus error reporting.

Figure 1. MVME204 Functional Block Diagram


RAM ARRAY
4 ROWS OF 4 BYTES
64K RAMS = 1Mb
MULTIPLEXED ADDRESS
ADDRESS DECODE AND MULTIPLEXING
64-BIT ARRAY BUS
PARITY BITS
PARITY BUFFERS
PARITY ERROR DETECTION
TIMING AND CONTROL
32-BIT DATA BUS
32-BIT ADDRESS BUS
MVMX32bus INTERFACE
VMEbus INTERFACE
MVMX32bus
VMEbus

MVME204 STATUS/CONTROL REGISTER FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
PE	RP	PR1	PR0	PRBEREN	MCACHE	WWP	EPER

PE: <Parity Error> The MVME204 status bit, when set indicates that a parity error has occurred from a VMEbus or MVMX32bus read access. It can be cleared by writing a zero from the VMEbus or can be set for diagnostic purposes.

RP: <MVMX32bus Private> When set, RP disables any VMEbus access to the MVME204 DRAM array.

PR1,0: <Private RAM> PR1 and PR0 allocates the MVME204 DRAM array area to the VMEbus shown by the following table. These bits are "don't cares" when the RP bit is set.

PR1,0	Memory Segment VMEbus Accessible
0 0	3, 2, 1, 0
0 1	3, 2, 1
1 0	3, 2
1 1	3

PRBEREN: <Private Bus Error Enable> When set, PRBEREN causes a Bus Error to be issued to the VMEbus device attempting to access memory that has been allocated private to MVMX32bus by the PR1,0 bits, or the RP bit of the MVME204 Control Register.

MCACHE: <Memory Cacheable> When set allows the MVMX32bus port to be cached by the MVME130 system. MCACHE enables assertion of MCACHE* on the MVMX32bus with the same timing as MASACKO, 1*. Indicating that the selected memory is cacheable.

WWP: <Write Wrong Parity> When set, causes the wrong parity to be written to the addressed location for diagnostic purposes.

EPER: <Enable Parity Error Report> When set, allows the MVME204 error detecting circuitry to report errors to the selecting device. Errors are indicated by the BERR* or MERR*. The PE bit in the MVME204 status/control register will not be afaffected by EPER. The PE bit will always indicate an error if one occurs.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Characteristics	Specifications
Power Requirements	MVME204 — +4.75 to 5.25 Vdc @ 5 A (max)
Operating Temperature	0° to 55°C
Storage Temperature	-40° to 85°C
Relative Humidity	5% to 95% (non-condensing)
Physical Dimensions Height Width Thickness	 9.25 in. (23.50 cm) 14.50 in. (36.83 cm) 0.60 in. (1.52 cm)
Storage Capacity	1Mb
Data Transfer Size	8, 16, 32 bits
Error Detection	Odd Byte Parity
Data Input/Output	32-bit VMEbus/MVMX32bus data
Input Address	32-bit VMEbus/MVMX32bus addressing

ORDERING INFORMATION

Part Number	Description
MVME204	VMEmodule 1024Kb Dynamic RAM with Byte Parity. Includes User's Manual.
MVME204/D1	VMEmodule Dynamic RAM User's Manual.

RELATED PRODUCTS

Part Number	Description
MVME130	VMEmodule 32-bit Monoboard Microcomputer with MC68020 CPU and MVMX32bus. Includes User's Manual.
MVME131	Same as MVME130 but also includes Memory Management Board.
MVME214	Static RAM/ROM VMEmodule with MVMX32bus. Includes User's Manual.

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GENERAL INFORMATION

1.1. INTRODUCTION

This manual provides general information, functional description, installation instructions, operating instructions and maintenance information for the MVME202, MVME222-1 and MVME222-2 Dynamic Memory modules.

Figure 1.1 shows the MVME202 module.

1.2. SPECIFICATIONS

The specifications of the MVME202, MVME222-1 and MVME222-2 Dynamic Memory modules are given in the following table.

Table 1.1: MVME202/222 Specifications

CHARACTERISTIC	SPECIFICATION
Memory Capacity	MVME202: 512K bytes (524288 bytes) MVME222-1: 1M bytes (1048576 bytes) MVME222-2: 2M bytes (2097152 bytes)
VMEbus Interface	Option A24:D16 slave interface, supporting 8-bit and 16-bit read, write and read-modify-write data transfers. Address modifier codes factory-programmed or user-selectable.
Access Times	Write access time (AS* to DTACK*): 70 ns (typ) Read access time (AS* to DTACK*): 320 ns (typ)
Error Detection	Byte parity generation and checking.
Memory Refresh	Local asynchronous refresh controller independent of VMEbus signals.
Indicators	LEDs on the front panel for parity error and board selection.
System Requirements	The following system modules are required to operate the MVME202/222 Dynamic Memory module: - a VME microprocessor module with an option A24:D16 VMEbus master interface - a VMEbus backplane - a VME card cage - a power supply unit

Table 1.1: MVME202/222 Specifications (continued)

CHARACTERISTIC	SPECIFICATION
Mechan. Dimensions	Double height VME board with front panel Board size: 233 mm * 160 mm Front panel size: 262 mm * 20 mm
Connectors	One 96 pole DIN 41612 connector for VMEbus
Power Requirements	+ 5 V DC, 1.4 A (typ), 1.9 A (max)
Environmental Conditions	Operating temperature: 0 to 70 C Storage temperature: -40 to 100 C Operating humidity: 0% to 90% non condensing

1.3. REFERENCE MANUALS

The following manuals may be used for further information about the VMEbus, and the VME system configuration:

- MVMEBS	VMEbus Specification Manual
- MVMECNFG1	VMEmodules Hardware and Software Configuration Manual

1.4. MANUAL TERMINOLOGY

1.4.1. Address and Data Formats

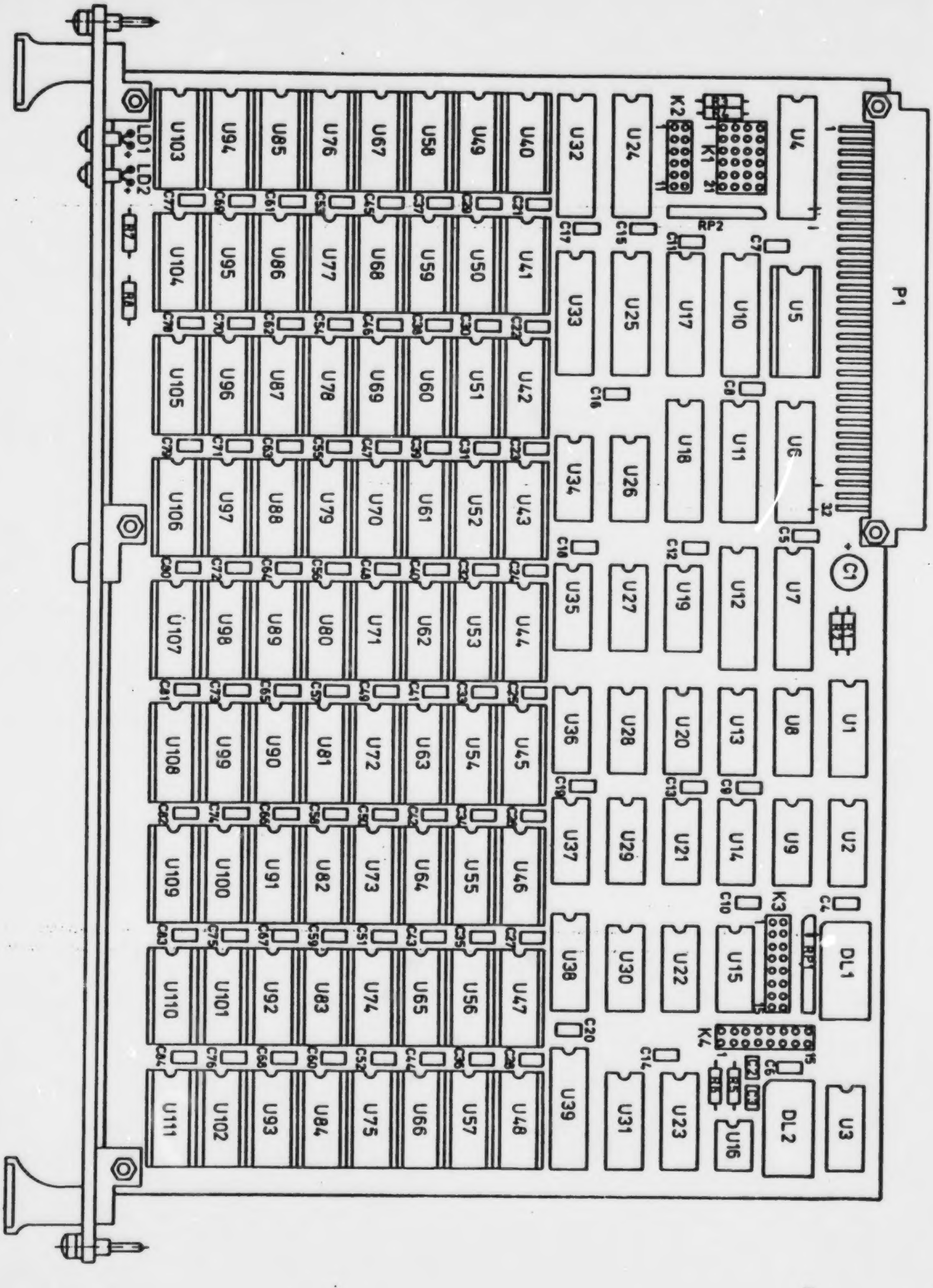
Throughout this manual, unless otherwise noted, all address and data values are given in hexadecimal format.

1.4.2. Electrical Signal Levels

A signal line is always assumed to be in one of two levels, or in transition between these levels. Whenever the term "high" is used, it refers to a high TTL voltage level (> +2.0 V). The term "low" refers to a low TTL voltage level (< +0.8 V).

There are two possible transitions which can appear on a signal line, and these will be referred to as "edges". A "rising edge" is defined as the time period during which a signal line makes its transition from a low level to a high level. The "falling edge" is defined as the time period during which a signal line makes its transition from a high level to a low level.

Figure 5.3. MVME202/222 Assembly Drawing



P1
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U5
U6
U7
U1
U2
U3
C1
DL1
DL2
K1
K2
K3
K4
RP1
RP2
LD1
LD2
U8
U9
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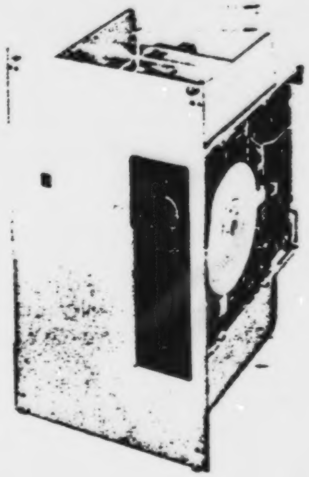
MOTOROLA
MICROSYSTEM PRODUCTS
TECHNICAL DATA

MVME820
MVME821
MVME822

Advance Information

VMEmodule™ VMEbus Plug-In Mass Storage Modules



STANDARD FEATURES

- All modules consist of standard 5-1/4" mass storage units (Winchester drives, floppy drives, etc.) mounted in an enclosure which plugs into a VME943 chassis
- All units include the MVME702 Disk Interface Module and necessary cabling for simple interface to VMEbus via the MVME320 Disk Controller

MVME820

- 15Mb (formatted) 5-1/4" Winchester Disk Drive (ST506 Interface)
- 650Kb (formatted) 5-1/4" double-sided, double density, 96 TPI, floppy disk drive

MVME821

- Two 650Kb (formatted) 5-1/4" double-sided, double-density, 96 TPI, floppy disk drives

MVME822

- 40Mb (formatted) 5-1/4" Winchester disk drive (ST506 Interface)
- 650Kb (formatted) 5-1/4" double-sided, double density, 96 TPI, floppy disk drive

Add mass storage capacity to a MVME943-based VMEbus system using any of three new mass storage modules: MVME820, MVME821 or MVME822. Each is supplied as a complete enclosed unit ready to be mounted in the right front side of the MVME943 Chassis by means of top and bottom rails that slide into four heavy-duty card guides provided in the chassis for this purpose. Four captive screws on the VME-type double-high front panel retain the storage unit.

Disk Drive Assembly MVME820 contains a 15Mb (formatted) 5-1/4" Winchester disk drive and a 650Kb (formatted) 5-1/4" double-sided, 96 TPI, floppy disk drive.

Disk Drive Assembly MVME821 contains two 5-1/4" double-sided, double-density, 96 TPI, floppy disk drives.

Disk Drive Assembly MVME822 contains a 40Mb (formatted) 5-1/4" Winchester disk drive and a 650Kb (formatted) 5-1/4" double-sided, double-density, 96 TPI, floppy disk drive.

A mass storage unit (less interface module) comprises a physical drive assembly and a PCB assembly which provides an industry-standard interface allowing up to four 5-1/4" drive units to be connected to a single formatter/controller. Maintenance is simplified by all hard disk electronic components being located outside the head/disk assembly.

Supplied with each mass storage module is a double-high disk interface module designed for mounting anywhere in the rear of the MVME943 chassis. The interface module greatly simplifies the task of connecting the MVME320 Disk Controller to a mass storage module and also facilitates the addition of other hard and floppy disks. When additional storage is added, standard 34-pin and 50-pin cables can be used.

WINCHESTER HARD DISKS

The CM5619 hard disk supplied with the MVME820 Plug-In Storage Unit was chosen from the CM5000 Series of 5-1/4" Winchester Disk Drives manufactured by Computer Memories Inc. of Chatsworth, CA. This series utilizes a Winchester-type head/media technology similar to that of IBM-3350 type disk drives.

This document contains information on a new product. Specifications and information herein are subject to change without notice.
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The CM5619 disk drive utilizes three platters having two data surfaces apiece. Each data surface has one movable head to service the 306 data tracks. Both the dc operating voltages required by the CM5619 and its outline dimensions are consistent with those of industry-standard minifloppy disk drives.

Mechanical and contamination protection for the CM5619 heads, actuator and disks are provided by an impact resistant aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron filter. A breather filter equalizes internal/ambient air pressures without chance of contamination.

The Model 1304 hard disk supplied with the MVME822 Plug-In Storage Unit was chosen from the 1300 Series of 5-1/4" Winchester Disk Drives manufactured by the Micropolis Corporation of Chatsworth, CA.

The 1304 disk drive utilizes four disks and six data surfaces having a total of 4980 physical tracks. When MFM recording format is used, 8192 bytes per track or 32 sectors per track (256-byte sectors) are obtained. Each of the six movable heads services 830 data tracks.

A "chassis-within-a-chassis" design utilizes a die cast drive assembly suspended within a die cast outer frame to provide maximum isolation against mechanical vibration and shock. An active air filtration system utilizes a 0.3 micron filter and another 0.3 micron filter insures contamination-free equalization of pressures between the clean area and the external environment.

HARD DISK DRIVE FEATURES

- Storage Capacities:
  - — MVME820 — 19.14Mb unformatted, 15Mb formatted
  - — MVME822 — 51.90Mb unformatted, 40Mb formatted
- Reliable Winchester Design
- Standard Minifloppy Outline/mounting
- Transfer Rate — 5Mbits/second
- Brushless DC Spindle Motor
- Electronic Damping

FLOPPY DISK DRIVE

The floppy disk supplied with the MVME820, MVME821, and MVME822 Plug-In Mass Storage Modules was selected from the FD-55 series of LSI mini-flexible disk drives manufactured by The TEAC Corporation of America of Montebello, CA. The model chosen: FD-55F, is a 5-1/4", soft sector, FM/MFM version of industry standard outline and half height — 1.63".

FLOPPY DISK DRIVE FEATURES

- Storage Capacity:
  - — 650Kb, Formatted, MFM Mode
- Data Transfer Rate — 250Kb/s (MFM)
- Average Access Time — 94 ms
- Track Access Time — 3 ms
- Settling Time — 15 ms
- Tracks Per Disk — 160
- Track Density — 96 Tracks Per Inch

CONTROLLER — DISK DRIVE — INTERFACE MODULE CONNECTIONS

MVME820/MVME822 CABLING

Hard disk data signals are conducted between MVME320 Disk Controller jack J2 and jack J2 on the MVME820 or MVME822 Hard Disk Drive via the provided 20-line flat ribbon cable. The provided Y-cable, which has two 50-pin connectors and lines 1 through 34 brought out to a 34-pin connector, is used for conducting control and data signals between the disk controller, the 5-1/4" hard disk drive and the disk interface module for connection (by separate cable) to the storage assembly's floppy disk and (optionally) to additional floppy or hard disk drives. One 50-pin end of the Y-cable is connected to jack J2 on the MVME320 Disk Controller and the 34-pin connector to J1 on MVME820 or MVME822. The other 50-pin end is connected to J9 on the interface module. Control and data signals are sent to the 5-1/4" floppy disk drive by connecting the provided 34-conductor cable between jack J10 on the interface module and jack J3 on the disk drive.

Facilities for connecting additional mass storage to the MVME320 Disk Controller are also provided by the interface module. Additional 5-1/4" or 8" hard disks and 5-1/4" or 8" floppy disks are connected to the interface module using standard 20-, 34- and 50-conductor cables, as required. Should additional storage beyond that provided by the MVME820 or MVME822 Plug-In Modules not be required or should the user not use the interface module, a custom 50-conductor cable can be fabricated for connecting jack J3 on the disk controller to jacks J1 and J3 on the hard and floppy disk drives, respectively.

MVME821 CABLING

Connections between the disk controller and the dual 5-1/4" floppies of the MVME821 Plug-In Module are made using the supplied 50-conductor cable which is connected between J3 on the controller and J9 on the interface module. To complete transmission to the floppy disk drives of data and control signals which reach the interface module via the 50-conductor cable, the supplied 34-conductor Y-cable is connected between jacks J10 on the interface module and J3 on each floppy drive.

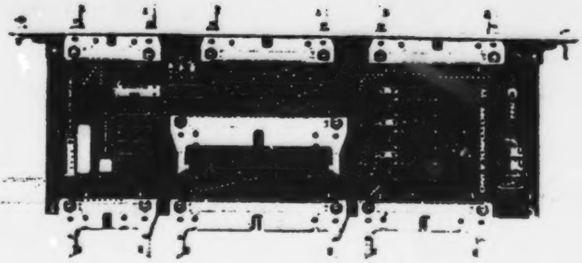
For the MVME821 as well as the MVME820 and MVME822 Plug-In Modules, facilities for connecting additional mass storage to the MVME320 Disk Controller are provided by the interface module. Additional 5-1/4" or 8" hard disks and 5-1/4" or 8" floppy disks can be connected to the interface module using standard 20-, 34- and 50-conductor cables, as required. Should additional storage beyond that provided by the MVME821 Plug-In Module not be required or should the user not use the interface module, a custom 50-conductor cable can be fabricated for connecting jack J3 on the disk controller to the J3 jacks on the two floppy disk drives.

DISK INTERFACE MODULE

Designed for mounting anywhere along the back of the MVME943 Chassis (or standalone use), the MVME702 Disk Interface Module supplied with each of the three storage modules extends the functions of the MVME320 Disk Controller by:

1. Organizing the controller's data and control output signals into the conventional groups required for interfacing hard and floppy disk drives;
2. Buffering and terminating the 5-1/4" hard disk control signals output from the controller;
3. Providing jumper headers which permit configuring for the quantity and types of hard and floppy disk drives required for an application.

All capabilities of the MVME320 to control various combinations of 5-1/4" and 8" hard and floppy disk drives are supported by the MVME702 Disk Interface Module.



PLUG-IN STORAGE MODULE SPECIFICATIONS

Characteristics	Specifications
Power Requirements	
Voltage	12 Vdc +5%
Current at 12 Vdc	
MVME820	1.93 A (typ) 4.4 A (max)
MVME821	0.85 A (typ) 1.8 A (max)
MVME822	2.30 A (typ) 3.7 A (max)
Voltage	5 Vdc +5%
Current at 5 Vdc	
MVME820	1.34 A (typ) 1.6 A (max)
MVME821	0.88 A (typ) 1.2 A (max)
MVME822	0.90 A (typ) 1.5 A (max)
MVME702	0.38 A (typ) 0.48 A (max)
Environmental Limits	
Operating Temperature	0°C to +55°C
Storage Temperature	−40°C to +85°C
Humidity Range	5 to 90%, non-condensing
Mechanical Specifications	
Height x Width	
(front panel)	10.3" x 6" (262mm x 152mm)
(drive package)	9.6" x 5.4" (244mm x 137mm)
Depth	8.2" (208mm)
Height x Depth	
MVME702	9.2" x 3.2" (234mm x 81mm)
Thickness	
MVME702	0.5" (12.7mm)
Data Rates	
Winchester	5Mbits/second
Floppy	250Kbits/second

ORDERING INFORMATION

Ordering Number	Description
MVME820	Plug-In Mass Storage Unit — 15Mb Hard Disk Drive and MVME702 Disk Drive Interface Module assembly. Installs in MVME943 Chassis. Includes User's Manuals.
MVME821	Plug-In Mass Storage Unit — Two 650Kb Double Sided, Double Density, Half Height Floppy Disk Drives and MVME702 Disk Drive Interface Module assembly. Installs in MVME943 Chassis. Includes User's Manuals.
MVME822	Plug-In Mass Storage Unit — 40Mb Hard Disk Drive and MVME702 Disk Drive Interface module assembly. Installs in MVME943 Chassis. Includes User's Manuals.
MVME820/D	Plug-In Mass Storage Unit User's Manual.
MVME702/D	Disk Interface Module User's Manual.

RELATED DOCUMENTATION

MVME320/D	VMEbus Disk Controller Module User's Manual.
M68KVSWD1/D	VME/10 Microcomputer System Computer Memories Model CM5000 Series Winchester Disk Drive User's Manual.
M68KVSFD2/D	TEAC Model FD-55 Series Floppy Disk Drive User's Manual.
MVME943/D	VMEmodule Chassis User's Manual

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The MVME705 6-Channel Serial Transceiver Module provides the receiver and transmitter circuits for converting the input/output signals of the MVME331 and MVME333 Intelligent Communication Controllers to the RS232C and/or the RS422B standard for serial data communications. The MVME705 module is connected to the MVME331/MVME333 module via a DIN 41612 C64 connector and a 64 pole flat ribbon cable. Six standard, 25 pole subminiature-D connectors are mounted on the front panel for attachment of serial peripherals.

Each serial port connector can be configured independently as either Data Communcations Equipment (DCE) for connecting terminals, printers etc, or as Data Terminal Equipment (DTE) for connecting modems, host computers etc.

Each channel of the MVME705 module also can be configured separately for either the RS232C or RS422B standard. This is achieved by inserting either the RS232C or the RS422B transmitter and receiver devices into the on-board IC sockets and changing the position of jumpers. The MVME705 product package includes all components required for any desired configuration.

1.2 SPECIFICATIONS

The specifications for the MVME705 module are shown in Table 1.1.

1.3 REFERENCE MANUALS

The following documents may be used for further information concerning the MVME331 and MVME333 modules and the serial peripheral interfaces.

- MVME331 Intelligent Communication Controller User's Manual
- MVME333 Intelligent Communication Controller User's Manual
- MVMEBS VMEbus Specification Manual
- DL128 Motorola Linear and Interface Integrated Circuits Data Book
- RS232C EIA Standard
- RS422B EIA Standard

Table 1.1: MVME705 Module Specifications

CHARACTERISTIC	SPECIFICATION
General	Six channel line driver/receiver module for connection to the MVME331 and MVME333 Intelligent Communication Controllers via a 64 pole flat ribbon cable. The serial port signals are available at 25 pole connectors on the front panel.
Serial Port Characteristics	Each channel can be configured to either the RS232C or RS422B standards. The front panel connectors can be configured to either DCE or DTE.
Supported Signals	TXD - Transmitted Data RXD - Received Data RTS - Request To Send CTS - Clear To Send DSR - Data Set Ready DTR - Data Terminal Ready DCD - Data Carrier Detect TRXC - Transmitter-Receiver Clock RTXC - Receiver-Transmitter Clock
Dimensions	Double height / reduced depth VMEmodule Board size: 233 mm * 80 mm Front panel size: 262 mm * 40 mm
Connectors	One DIN 41612 C64 to MVME331/MVME333 module Six 25 pole sub-D serial port connectors
Power Requirements	+ 5 V DC, 1.5 A (max), 0.2 - 1.0 A (typ) +12 V DC, 150 mA (max), 0 - 110 mA (typ) -12 V DC, 150 mA (max), 0 - 110 mA (typ) Typical values are dependent upon configuration
Environmental Conditions	Operating temperature: 0 to +55 deg C Storage temperature: -40 to +100 deg C Operating humidity: 0 to 90% non condensing
Shipment Configuration	All channels configured as RS232C DCE for terminal connection. 330 pF capacitors installed for slew rate limitation and noise filtering.
Included in Shipment	- Six sets of RS422B transmitter and receiver ICs (MC3487 and MC3486) - Thirty 100 Ohm termination resistors - One interconnection cable to MVME331/MVME333

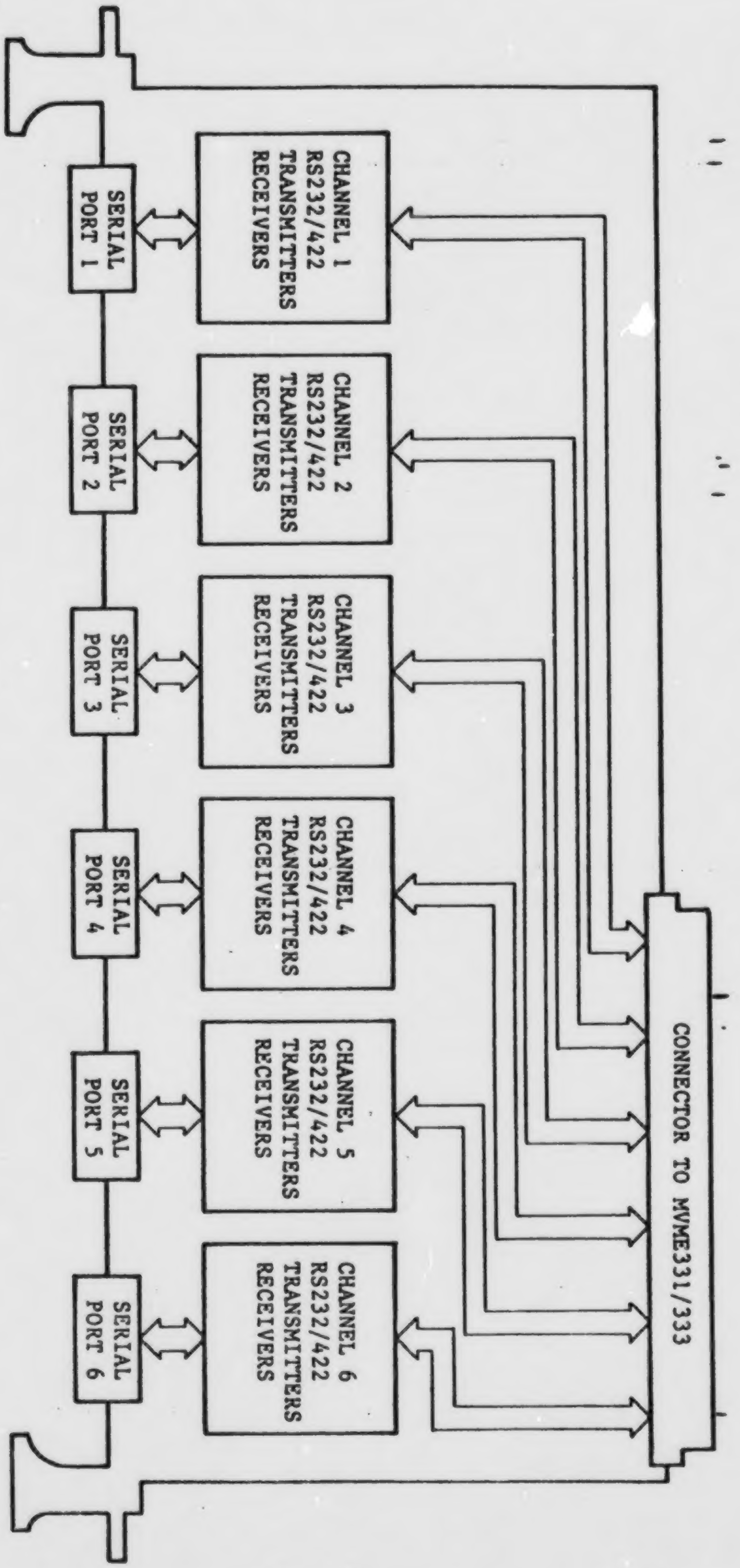


Figure 2.1: MVME705 Block Diagram

CHANNEL 1
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 1
CHANNEL 2
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 2
CHANNEL 3
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 3
CHANNEL 4
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 4
CHANNEL 5
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 5
CHANNEL 6
RS232/422
TRANSMITTERS
RECEIVERS
SERIAL PORT 6
CONNECTOR TO MVME331/333

IMAGRAPH

VME GRAPHIC PLUS SERIES

1280 X 1024 X 4/8 + 2 ADVANCED COLOR GRAPHIC CONTROLLERS FOR VME BUS

- **Flicker Free Display Output**
  Display Resolution
  1280 x 1024 x 4/8 (+2)
  1024 x 1024 x 4/8 (+2)
  1024 x 768 x 4/8 (+2)
  640 x 480 x 4/8 (+2)
  512 x 512 x 4/8 (+2)
  Adressable Window
  2048 x 1024 x 4/8 (+2)
  Image Memory: 4/8 bits/pixel
  Integer Zoom x1-x16
  Pan, Scroll
  16 or 256 color/gray shades from 16.8M palette
  Overlay Memory: 2 bits/pixel
  Pan, Scroll without zoom
  Blink & Read mask
  Transparent or Opaque display of image
  4 colors from 16.8M palette
  Scan Rate:
  Non-Interlaced
  64 KHz Horizontal
  60 Hz Vertical

- **On Board VLSI Graphic Processor**
  Hitachi ACRTC HD-63484 with 1.3 million pixels per second drawing speed or 32,500 vectors/second (40 pixels vector)

- **Standard Video Output**
  RGB Analog, RS343
  9 pin D-shell
  Cable optional

- **Basic Graphic Instructions**
  Pixel, Line, Arc, Circle
  Ellipse, Polygon,
  Split screens

- **Enhanced Graphic Instructions**
  Pattern Fill, BIT-BLT operations
  Hardware clipping,
  Boolean Read Modify Write drawing commands
  Windows via overlays
  Hardware write mask for all functions

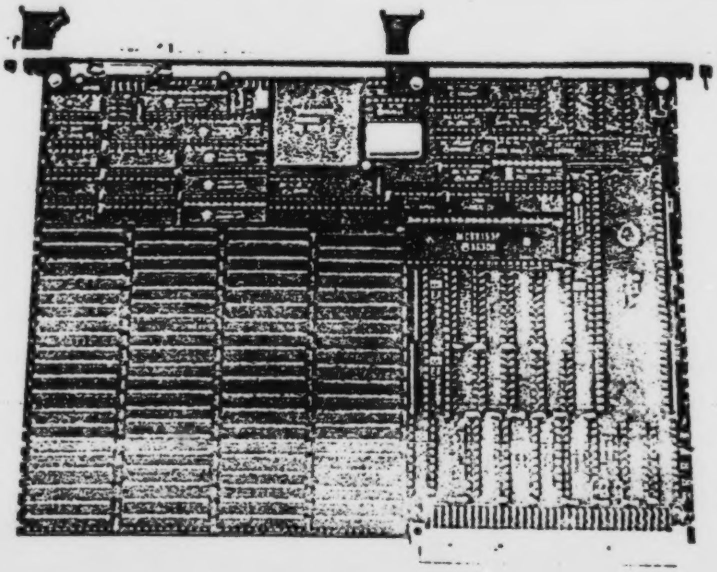
- **Advanced Architecture**
  True dual port memory mapping
  Image memory transfers up to 4.4 million 8 bit/pixel/second in the burst mode
  Overlay memory transfer up to 17.7 million 2bit/pixel/second
  On board software programmable interrupt controller
  Option to have up to 4 Imagraph boards in same address space, using address modifiers
  DTB slave, A24, D16

- **Physical Board Dimension**
  Single slot height
  Double width Eurocard format

The VME 1280-10 is a state-of-the-art, high resolution, high performance color graphic board for VME bus based computers. The VME 1280-10 is designed for applications including CAD, CAE, graphic arts workstations, presentation graphics, scientific/industrial instrumentation, display and process control graphics.

The VME 1280-10 contains 2.5 MByte of on-board display memory, which provides a display window of 1280 X 1024 X 4/8 + 2. A total of 256 colors/gray shades can be displayed simultaneously from a programmable palette of 16.8 millions. The video output is at 60 Hz non-interlaced which allows CRT displays to be flicker free. The advanced open architecture of the VME 1280-10 is based on a new generation of VLSI graphic controller, the Hitachi ACRTC HD-63484. Combined with the 256K (64X4) Video RAM technology, the VME 1280-10 achieves a performance spec that is 5 to 10 times faster than NEC 7220 based controllers; and 2 to 5 times faster than similar Hitachi HD-63484 based designs that do not utilize Video RAM technology.

Software Drivers: Written in "C" language for OS/9, UNIX V, P DOS, Versados.



TECHNICAL DESCRIPTION

HIGH PERFORMANCE GRAPHIC ENGINE HD-63484

The IMAGE PLUS SERIES graphic controllers utilize the Hitachi HD-63484 ACRTC Advanced CRT Controller as its main engine. The HD-63484 contains an intelligent yet powerful drawing processor to accept graphic commands directly from the VME processor via I/O ports. Immediately, the commands are executed onto the image memory or the overlay display memory. No waiting time for horizontal or vertical retrace is required for pixel drawing and no pixel update flash will be observed even at 1280 x 1024 x 4/8 + 2, 60 Hz refresh rate, 106 MHZ bandwith. Hence the overall execution through-put is greatly increased. Simple commands from line, arc, ellipse, polygon, zoom 1-16x(image memory only) pan, and scroll to enhanced commands such as pattern fill, hardware window clipping and BIT-BLT can all be swiftly executed.

DUAL PORT MAPPING SPEEDS PIXEL ACCESS

The entire image & overlay memory (up to 2.5 MBytes) is designed to support independent accesses either by the HD-63484's drawing processor or the host VME processor. The VME bus will accept transfer of 16 bits/word, which is equivalent to 2 horizontal 8 bit pixels, at a transfer rate of 450ns/word or 4.4 million 8 bit pixels per second. In the overlay addressing mode, a 16 bit word is equivalent to 8 horizontal 2 bit pixels or a transfer rate of 17.7 million pixels/second.

HIGH RESOLUTION FORMATS

The VME Graphics Plus Series boards are available in various formats depending upon the amount of memory with a maximum of 2.5 Mbytes of on-board display memory. Up to 2 MBytes of memory can be utilized for 2048 x 1024 x 8 addressable image memory. Active image display windows are available from 1280 x 1024 x 4/8 + 2 to 512 x 512 x 4/8 + 2 bits/pixel.The additional .5 Kbyte of memory is used for an addressable 2048 x 1024 x 2 overlay. Corresponding active overlay memory display is available from 1280 x 1024 x 2 to 512 x 512 x 2 bits /pixel. With 1024 x 768 display resolution, double buffering is available. In the [illegible] x 1024 x 8 bit format, the entire 2 MByte memory is utilized for one page. When image memory is zoomed to a lower resolution format, only partial image memory is utilized; hence, additional non-display memory can be utilized for multiple page display, looping or panning. Since zoom is not available on the overlay memory, texts or graphics written in the overlay will not be affected when the base image memory is zoomed, panned or scrolled.

LOOK UP TABLE (LUT) & DIGITAL TO ANALOG CONVERTER (DAC)

The GRAPHIC PLUS SERIES is available with either Brooktree BT451 or BT458 RAM DACs. The BT451 displays 256 colors/16 gray shades from a LUT palette of 4096, whereas the BT458 will display 256 colors/gray shades from a LUT palette of 16.8 million. The LUT is designed with dual ported RAM. Programming of the LUT does not require waiting for vertical retrace, hence no possible related flashes on display. Both DAC options will support the 2 bit overlay, displaying up to 4 colors from the 4096/16.8 million palette. Additional functions such as programmable bit plane read, blink mask, transparent or opaque display of the image memory through the overlay memory graphics, are all standard features.

PROGRAMMING

The programming of any GRAPHIC PLUS SERIES board is fairly straightforward. The controller appears to the user as 11 memory mapped I/O registers + 2.5 MByte locations of memory. The registers are : 4 DAC registers, 2 HD-63484 registers, 2 Interrupt Controller registers, 1 board control register, 1 board status register, and 1 right mask register. I/O registers are mapped starting at the first location above memory. Once the registers are initialized with sets of proper values, all graphic commands are passed directly to the HD-63484 registers for interpretation and execution. The user can also access individual pixels directly as simple memory locations. The factory default board address is 800,000 HEX with memory starting at this base address. The Board Base Address is jumper plug changeable by the user.

SPECIFICATIONS:

Display Resolution:
1280 x 1024 x 4/8 (+2 overlays)
1024 x 1024 x 4/8 (+2 overlays)
1024 x 768 x 4/8 (+2 overlays)
640 x 480 x 4/8 (+2 overlays)
512 x 512 x 4/8 (+2 overlays)

Addressable Resolution
- Up to 2048 x 1024

Look Up Table-Brooktree BT458/BT451
- Blink, overlay disable
- Transparent or Opaque Overlay
- Image memory display 256 colors/gray shades from 4096/16.8M
- Overlay memory display 4 colors from 4096/16.8M

Output Video
- RGB analog with sync on green, RS343
- 9 pin D-shell cable option

On-Board Memory
- Up to 2 MBytes high speed video RAM + 0.5MB for overlays
- Accessible via VME bus or by Hitachi drawing processor
- Write mask register for all bit planes & graphic functions

Dual Port Memory Access
- Jumper selectable
- Direct memory mapped scheme in 2.5MBytes + 128KBytes for I/O register
- Maximum Average Transfer Rate
  Image memory: 450ns per word or 4.4 million 8 bit/pixels/second
  Overlay memory: 17.7 million 2 bit pixels per second

High Speed Graphic Graphic Functions (HD-63484)
- Line, rectangle, arc, circle, polygon, ellipse
- Hardware integer Zoom x1-x16, independent X,Y (no zoom on overlays)
- Hardware pan, scroll of zoomed image memory
- Hardware line scroll of non-zoomed overlay
- Three horizontal split screens
- Pattern fill, BIT-BLT
- Hardware clipping
- Boolean read modify write drawing commands
- 1.3 million pixels/sec continuous drawing speed

Interrupter
- 7 VME bus interrupt levels-software selectable
- Interrupt conditions
  ACRTC command/FIFO status
  V sync (can be polled)

Bus
- VME P1, A24, D16, vectored interrupts
- Address Modifier 10-1F Hex
- Single or Multi-processor environment

Physical Dimension
- 233 mm x 160 mm double width Eurocard

Power Consumption: +5v @ 4.5 Amp

Environment
- Relative Humidity 0 - 90% (noncondensing)
- Operating Temp 0 - 55 degrees C

Warranty: 1 year factory parts and labor

Specifications subject to change without notice

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APPENDIX D - SINADS SOFTWARE DETAILS

The SINADS program is organized in a number of tasks. The data and command transfer between tasks is organized via input and output queues, which are lists of memory addresses. The SINADS software tasks, queues, and structure of the data and command flow is described in the following paragraphs.

d1. SINADS Tasks

SINADS software consists of the following tasks:

a) RANGE task;
b) GYRO task;
c) OBSERVATION-PROCESSING task;
d) POSITION task;
e) DATAFLOW task;
f) ALARM task;
g) CHART task;
h) BOXES task;
i) GRAPHEXEC task;
j) EXEC task;
k) MENU task;
l) RADAR task; and
m) VESSEL task

Each task is briefly described in the following paragraphs.

d1.1. RANGE Task

The RANGE task reads the microwave range data from its input queue, and checks that no digits have been lost or added in transmission. If the range is in a correct format this task places it in the range output queue which can be read by other tasks.

d1.2. GYRO Task

The GYRO task reads the gyro data from its input queue, and checks that no digits have been lost or added in transmission. It also checks that the gyro reading number is within a range of between 0° and 360°. If the gyro reading is in the correct format it is placed in the gyro output queue for access by other tasks.

d1.3. OBSERVATION-PROCESSING Task

The OBSERVATION-PROCESSING task receives gyro data, microwave range data and previous position data. This information is used to check the observations for correctness and to adjust ranges for scale and slope. The processed observations are then placed into the observation task output queue to be used by the position task.

d1.4. POSITION Task

The POSITION task calculates a new position from received observation data. The new position is then placed in the position output queue and distributed by the DATAFLOW task.

d1.5. DATAFLOW Task

The DATAFLOW task keeps a list of all links between input queues and output queues. DATAFLOW checks all output queues to determine if they contain any new data. If there is new data, the DATAFLOW task places it into all input queues linked to a particular output queue.

d1.6. ALARM Task

The ALARM task keeps a list of all active alarms. As commands are processed this list is adjusted. The ALARM task receives commands from the MENU task requesting information. When a command is send to activate an alarm, the ALARM task changes the color of the alarm and displays the alarm message on the screen.

d1.7. CHART Task

The CHART task performs the scrolling and zooming of the chart. This task also toggles the screens between two VRAM buffers to achieve the scrolling effect, and controls the drawing of the routes, stations, and markers.

d1.8. BOXES Task

The BOXES task updates all screen alpha boxes as the new data comes into its input queue. The cursor box is updated every time this task is given time to run. The BOXES task also receives commands from the MENU task to change the contents of each box or the size of characters.

d1.9. GRAPHEXEC Task

The GRAPHEXEC task monitors the vessel position and sends a command to scroll to the CHART task. It also receives commands from the MENU task that effect the charts. The GRAPHEXEC task forwards these commands to the CHART task.

d1.10. EXEC Task

The EXEC task coordinates the startup of every other task. It controls which tasks are started depending on the operation mode selected by the user.

d1.11. MENU Task

The MENU task reads the keycodes from the keyboard buffer and processes them according to the function they call. This task also changes the menus on the screen in response to the key that has been pressed.

d1.12. RADAR Task

The RADAR task controls the radar scan converter to match the vessel heading and maintain a northup display. The RADAR task also changes the radar scale to match the chart scale and adjusts the radar controls.

d1.13. VESSEL Task

The VESSEL task receives the latest vessel position and gyro reading via its input queue. This data is used to draw the vessel in the correct position and orientation on the screen.

d2. SINADS Queues

SINADS uses data-queues for transfer of data between tasks and command-queues for transfer of commands between tasks. The queues are described in the following paragraphs.

d2.1. Data Queues

The following input and output data queues are used:

INPUT DATA QUEUES	OUTPUT DATA QUEUES
RANGE_INPUT_QUEUE	RANGE_OUTPUT_QUEUE
OBSERVATION_INPUT_QUEUE	OBSERVATION_OUTPUT_QUEUE
GYRO_INPUT_QUEUE	GYRO_OUTPUT_QUEUE
POSITION_INPUT_QUEUE	POSITION_OUTPUT_QUEUE
GRAPHEXEC_INPUT_QUEUE	
BOXES_INPUT_QUEUE	
VESSEL_INPUT_QUEUE	
RECORD_INPUT_QUEUE	

d2.2. Command Queues

The following command queues are used by SINADS software:

ALARM_COMMAND_QUEUE
BOXES_COMMAND_QUEUE
CHART_COMMAND_QUEUE
GRAPHEXEC_COMMAND_QUEUE
GYRO_COMMAND_QUEUE
MENU_COMMAND_QUEUE
OBSERVATION_COMMAND_QUEUE
POSITION_COMMAND_QUEUE
RANGE_COMMAND_QUEUE
TARGET_EXEC_COMMAND_QUEUE
VESSEL_COMMAND_QUEUE
(Radar)MESSAGE_CLERK_COMMAND_QUEUE
(Radar)RADAR_COMMAND_QUEUE
(Radar)TARGET_TRACKING_COMMAND_QUEUE
(UNIX)MESSAGE_CLERK_COMMAND_QUEUE
(UNIX)RADAR_COMMAND_QUEUE

d3. SINADS Data Flow

The flow of data within SINADS is managed by the DATAFLOW task. The DATAFLOW task keeps a list of all links between input queues and output queues and checks all output queues to determine if they contain any new data. If there is new data, the DATAFLOW task places it into all input queues linked to a particular output queue. The SINADS data flow diagram is shown in figure 2. The description of the diagram can be found in the following paragraphs.

d3.1. Range Data

The microwave positioning system range data is routed through the DATAFLOW task into the RANGE_INPUT_QUEUE. The RANGE task rejects data that are not in a correct format. All the remaining data is placed into the RANGE_OUTPUT_QUEUE. From there the range data is distributed by DATAFLOW task to the OBSERVATION_INPUT_QUEUE and the RECORD_INPUT_QUEUE.

d3.2. Gyro Data

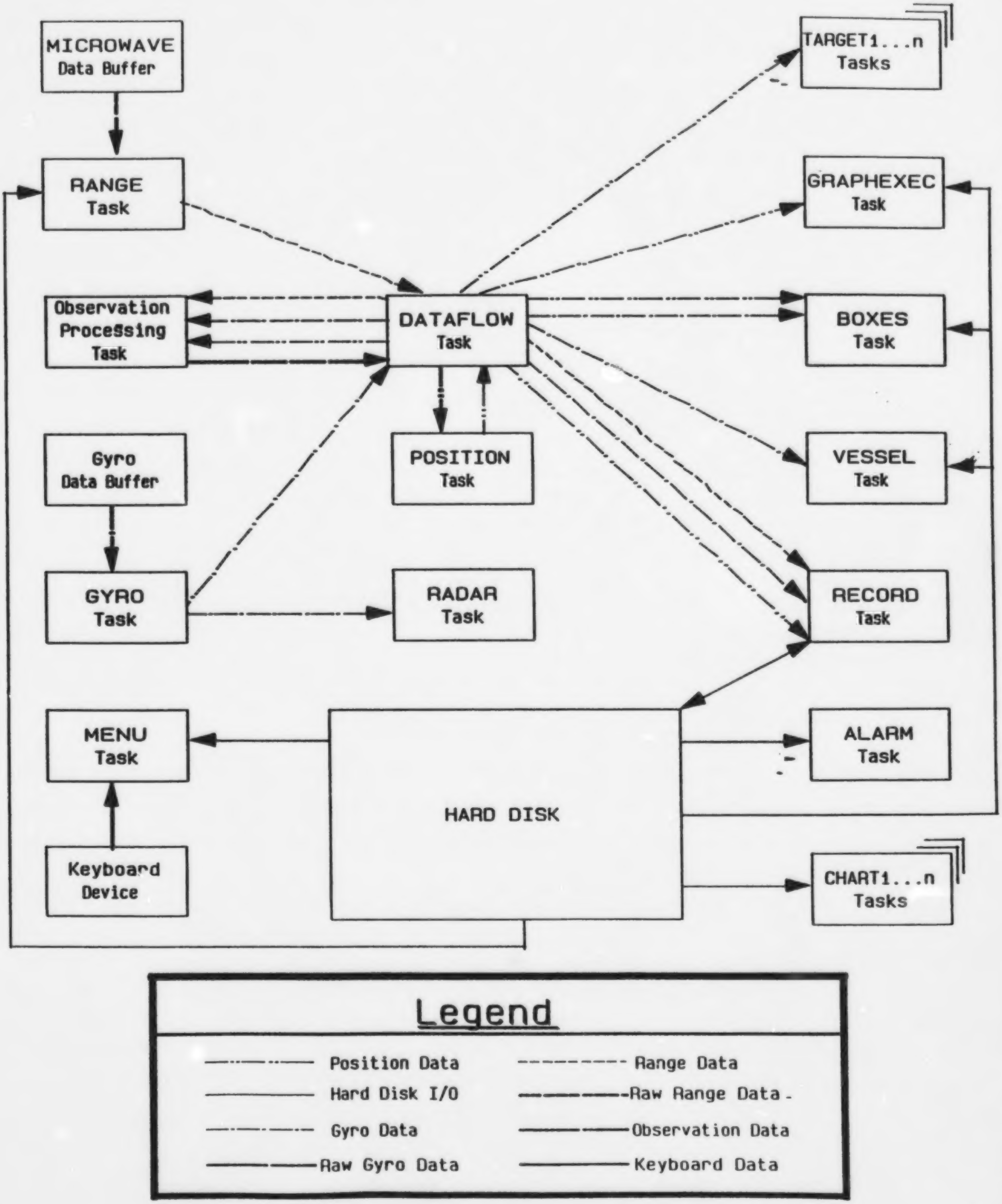
The gyro data is routed through the DATAFLOW task into the GYRO_INPUT_QUEUE. The GYRO task rejects data that are not in the correct format. The GYRO task places all properly formatted readings into the GYRO_OUTPUT_QUEUE and also sends this data to the RADAR task. The gyro data in the GYRO_OUTPUT_QUEUE are then distributed by DATAFLOW task to OBSERVATION_INPUT_QUEUE, RECORD_INPUT_QUEUE, BOXES_INPUT_QUEUE, and the VESSEL_INPUT_QUEUE.

d3.3. Observation Data

The observation data is calculated by the OBSERVATION-PROCESSING task and placed in the OBSERVATION_OUTPUT_QUEUE. DATAFLOW redirects this information to the POSITION_INPUT_QUEUE. The observation data is used by the POSITION task to calculate a new position.

SINADS DATA FLOW DIAGRAM

Figure 2


MICROWAVE Data Buffer
RANGE Task
Observation Processing Task
DATAFLOW Task
POSITION Task
Gyro Data Buffer
GYRO Task
RADAR Task
MENU Task
Keyboard Device
HARD DISK
TARGET1...n Tasks
GRAPHEXEC Task
BOXES Task
VESSEL Task
RECORD Task
ALARM Task
CHART1...n Tasks
Legend
Position Data
Range Data
Hard Disk I/O
Raw Range Data
Gyro Data
Observation Data
Raw Gyro Data
Keyboard Data

d3.4. Keyboard Data

The MENU task receives the keyboard data directly from the custom keyboard. These keyboard data is not passed through the DATAFLOW task.

d3.5. Hard Disk Data

The SINADS hard disk is used to store the configuration and data files. A number of tasks read the configuration files from the hard disk. A majority of data files are stored by RECORD and MENU tasks. The configuration and data files stored on the hard disk are listed below.

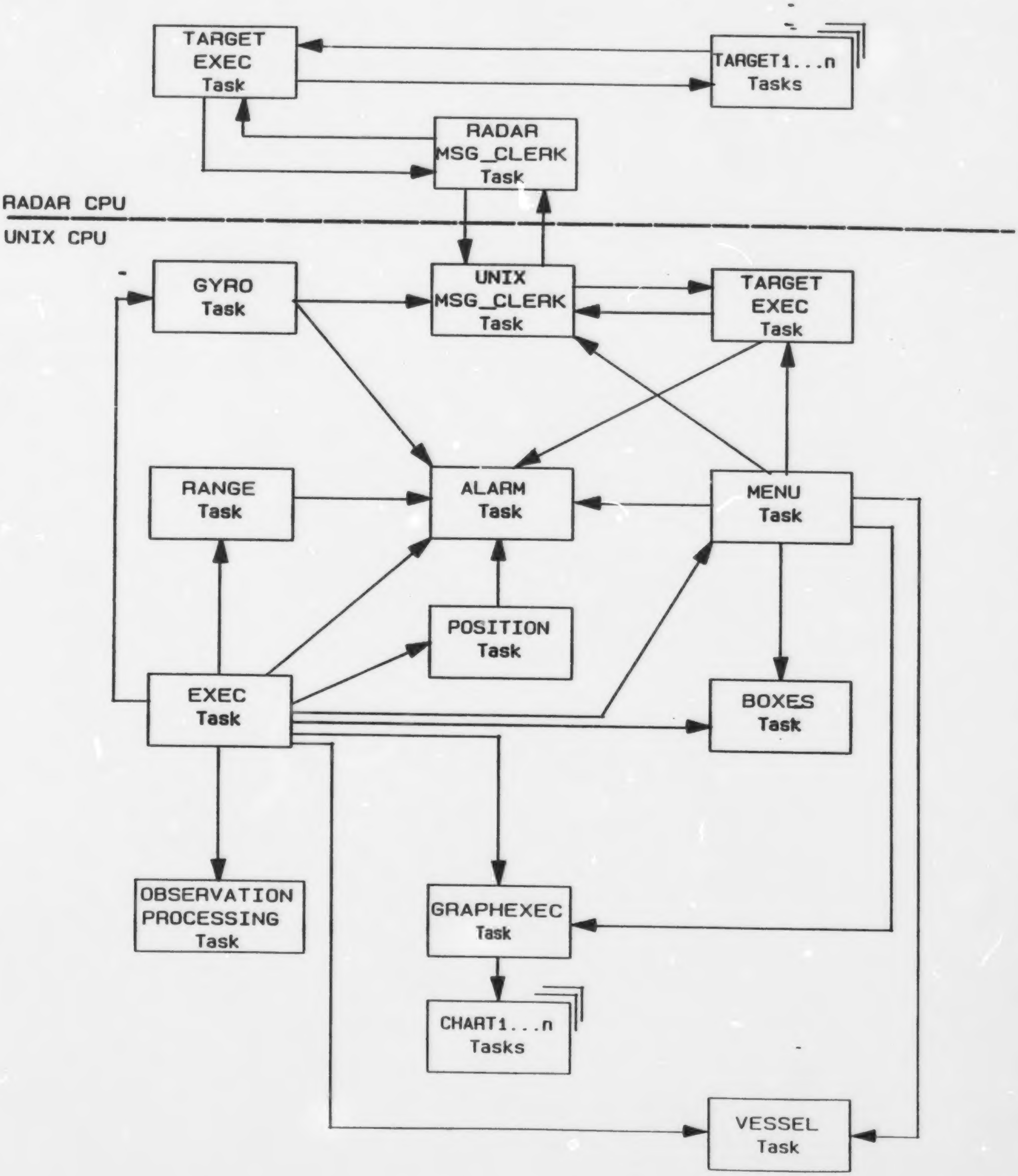
TASK	FILE DESCRIPTION
MENU	Menu key file
	Route file
	Station file
	Startup Parameters file
	Chart files
RECORD	Record Startup Parameters file
	Position data file
VESSEL	Vessel Shape file
BOXES	Boxes description file
GRAPHEXEC	Screen layout file
CHART	Chart files
ALARM	Alarm file

d.4. SINADS Command Flow

The SINADS command flow diagram is shown in figure 3. The description of the diagram can be found in the following paragraphs.

SINADS Command Flow Diagram

Figure 3


TARGET EXEC Task
TARGET1...n Tasks
RADAR MSG_CLERK Task
RADAR CPU
UNIX CPU
GYRO Task
UNIX MSG_CLERK Task
TARGET EXEC Task
RANGE Task
ALARM Task
MENU Task
POSITION Task
EXEC Task
BOXES Task
OBSERVATION PROCESSING Task
GRAPHEXEC Task
CHART1...n Tasks
VESSEL Task

d4.1. ALARM Task Commands

The ALARM task receives commands from all other tasks to activate an appropriate alarm. It receives commands from the MENU task to acknowledge alarms, silence alarms, disable alarms, or to show their status. The ALARM task also sends commands to the keyboard to activate the audible alarm.

d4.2. EXEC Task Commands

The EXEC task sends initialization commands to ALARM , POSITION , RANGE , OBSERVATION-PROCESSING, GYRO , VESSEL , BOXES , GRAPHEXEC and MENUS tasks.

d4.3. RANGE Task Commands

The RANGE task receives initialization command from the EXEC task. The RANGE task sends commands activating alarms to the ALARM task.

d4.4. POSITION Task Commands

The POSITION task receives initialization command from the EXEC task. The POSITION task sends commands activating alarms to the ALARM task.

d4.5. OBSERVATION Task Commands

The OBSERVATION-PROCESSING task receives the initialization command from the EXEC task.

d4.6. KEYBOARD Task Commands

The keyboard device receives commands from the ALARM task. The commands activate an audible alarm.

d4.7. GRAPHEXEC Task Commands

The GRAPHEXEC task receives initialization command from the EXEC task and commands relating to the chart manipulations from the MENU task. The GRAPHEXEC task also sends commands to the CHART task to initiate chart scrolling or to switch to a different chart.

d4.8. BOXES Task Commands

The BOXES task receives initialization command from EXEC task and commands relating to the manipulation of the alpha-boxes from the MENU task.

d4.9. MENU Task Commands

The MENU task receives initialization command from EXEC task. The MENU task sends alpha-box related commands to the BOXES task, alarm related commands to the ALARM task, radar related commands to the RADAR task, chart related commands to the GRAPHEXEC task, and vessel position related commands to the VESSEL task.

d4.10. RADAR Task Commands

The RADAR task receives commands from the MENU task.

d4.11. VESSEL Task Commands

The VESSEL task receives an initialization command from the EXEC task and vessel position related commands from the MENU task.

d4.12. GYRO Task Commands

The GYRO task receives an initialization command from the EXEC task.

APPENDIX E - SINADS CHARTS DATABASE

The SINADS chart database is based on a Triangular Irregular Network (TIN) rather than a simple vector structure.

The digitized data supplied in vector form is grouped into triangles, such that all data points from the chart are vertices of triangles. Colour information is associated with each triangle to facilitate the filled chart display algorithm.

The colour filled chart is generated by sampling the database at pixel location and obtaining the colour of the pixel from the colour of the triangle inside which this pixel lies. Horizontal groups of pixels of the same colour are then drawn as one line. The vertices of the triangles can have attribute data associated with them. This capability of TIN can be used for storage and selective display of navaids and other point-feature information.

The advantage of the TIN method is that chart drawing time is relatively independent of the current display scale. In addition, the TIN database allows for future development of continuous charts, and the implementation of the Graphical Information System (GIS) applications. The full implementation of TIN will allow to address ECDIS requirements.

A detailed description the TIN method can be found in [2].

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APPENDIX F - SINADS USER-INTERFACE

The SINADS user-interface provides a means whereby the user may control the system via directed syntax. It also provides the user with visual and audible feedback on the IDC screen and on the diagnostic ASCII terminal. The SINADS user-interface is a combination of the following hardware and software components:

a) high resolution RGB monitor;
b) custom membrane keyboard;
c) custom keyboard controller;
d) SINADS screen layouts;
e) directed syntax menus; and
f) diagnostic display ASCII terminal.

The SINADS user-interface components are described in the following paragraphs.

f1. High Resolution RGB Monitor

A HITACHI Model 4119DDL 19" colour RGB monitor was used for SINADS display. The monitor has a 1024 pixels x 768 lines resolution, and is equipped with an anti-glare screen. OSL modified the monitor chassis to include a custom membrane keyboard with back-lighting, a keyboard controller with power supply, AC power and degauss relays, alarm speaker, and a light hood. A monitor specification sheet and an IDC outline drawing Fig. 4 are attached at the end of this appendix.

f2. Custom Membrane Keyboard

To address the requirements of the SINADS user interface OSL designed and manufactured a custom membrane keyboard. The keyboard layout in illustrated in

Fig.5 and Fig.6 and the keyboard switch matrix schematics is shown in Fig.7 and Fig.8. The membrane keyboard is equipped with fluorescent backlighting for night operation.

f3. Custom Keyboard Controller

The SINADS keyboard controller scans the switch matrix of the custom keyboard in order to detect which key contact is being closed. Once a keypress is confirmed the controller decodes it, converts into an ASCII character, and sends via an RS232 port to the computing system. The keyboard controller receives commands from the computing system activating an audio alarm. The audio alarm sound sequences are stored in an EPROM on the controller board. The keyboard controller also activates 2 relays which allow turning the IDC on and off as well as the monitor degaussing using two special keys on the membrane keyboard. The programming manual for the keyboard controller is included at the end of this appendix.

f4. SINADS Screen Layouts

The prototype SINADS screen layout is illustrated in Figure 9 . In this configuration the chart is located on the left, and the alphanumeric information on the right hand side of the screen. The alarm messages area occupies the top of the screen and the directed syntax menu its bottom. The chart is a 640 pixels x 640 lines square. This size was selected to match the radar image from the RSC. The lower right corner of the chart area is used to display the chart scale. A horizontal bar located immediately below the chart indicates graphically the progress of building or changing the scale of the chart.

The directed syntax menu area is divided into eight boxes. Each menu label is centered in it's box. Above the menu boxes, alligned with the left edge of the screen, is a menu title indicating the currently used level of menus.

Alligned with the right edge of the screen is the system mode area, which informs
the user of the mode the system is in.
The top line of the screen contains the eight alarm categories. The categories change colors as alarms are activated and acknowledged.
The second line from the top is where the active alarm description is displayed.
The date and time is located at the end of the second line from the top.
The alphanumeric information is displayed in the alpha-boxes. There are 6 alpha-boxes in total. The first 4 boxes display any data chosen by the user. The 5th box is a dedicated cursor box which displays positioning information of the cursor. The 6th alpha-box is is used to display system status and warning messages. The examples of content of alpha-boxes are shown in Fig.10, 11,12 and 13. Although the prototype system provided only a single screen layout, SINADS was designed to provide multiple chart windows. Alternative screen configurations are shown in Fig. 14,15,16, and 17.

f5. Directed Syntax Menus

The user interface has been designed with configurable menus in mind, based on the design of the custom membrane keyboard. Each menu can be easily altered, added, or removed without any programming. This task requires that all menu labels and other information about each menu are external to the program code. A disk file contains the information about each menu and when the program starts, this file is read and used. To create this file a separate program is provided.

f5.1. Menu Format

SINADS menus use the following file format:

00000000000000 - menu location

CHART_MENU	- menu title
OFF	- menu key label { key 1 }
chart_onoff	- menu key function name
34	- menu key function index
FILLOFF	- menu key label { key 2 }
chart_fill_onoff	- menu key function name
35	- menu key function index
....	- etc for all eight (8) softkeys

Each menu consists of a location, menutitle, and 8 choices with a label, function name, and function index for each choice.

f5.2. Menu Location

Menu location identifies the menu position in relation to all the other menus.

eg. 0000000000238A

This menu is located at:

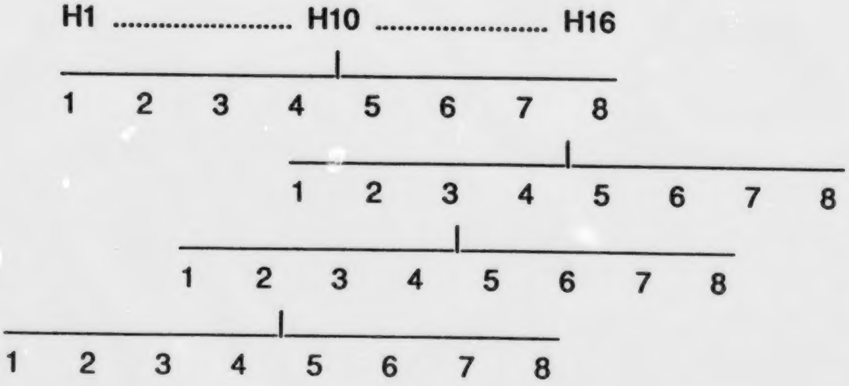
A - hardkey menu 10 (hexvalue of A).

8 - menu from key 8 from menu A.

3 - key 3 from menu key 8 from menu A.

2 - key 2 from menu key 3 from menu key 8 from menu A.

This type of setup allows the program to know that key 2 should point to this menu. The menu location for the above example can be presented in the following diagram:


H1 .... H10 .... H16
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8

f5.3. Menu Title And Label

Menu Title and Label contain strings of characters that describe the menu or the key choice. Each label should describe the function or action of the key. The title can often be used to ensure that the user understands the keys action.

f5.4. Function Name and Index

The function name allows the programmer to edit the menu file without the need for the function index table. The function index points to an array of function addresses that is created by the menu program and used by the navigation program. The function index allows the navigation program to obtain the function address without the necessity of hard-coding each function call. This enables configurable function calls depending on the user interface requirements in any specific application.

f5.5. User I/F Program

The menu file is read an placed in a menu structure. This structure is built at startup and will only allocate space for each menu, thus ensuring that no RAM space will be wasted.

f5.6. Menu Tree

The menu tree describes choices available to the user. This menu tree includes hardkeys as well as softkeys. The SINADS menu tree is shown on pages F-28,

F-29, and F-30. The SINADS Operator's Manual starting on page F-31 provides a detailed description of the SINADS menu tree.

f5.7. User-Interface Intertask Communications

Functions called by the user-interface place commands into queues of other tasks.

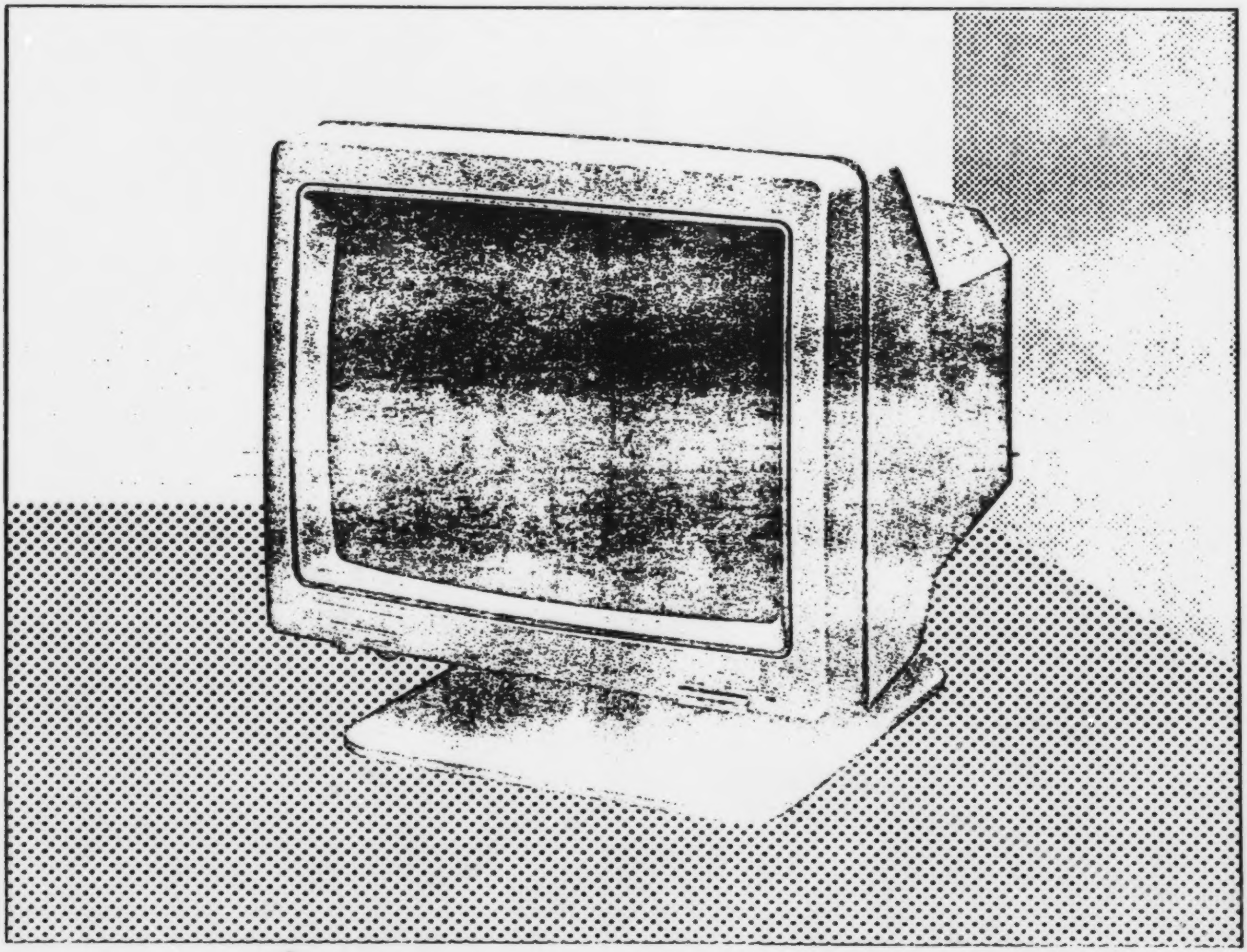
f6. Diagnostic Display ASCII Terminal

The SINADS diagnostic information is displayed on a monochrome ASCII terminal. The information includes real-time data related to the vessel positioning, radar target tracking, I/O functions, and chart manipulations. The diagnostic display is designed to help OSL personnel in troubleshooting and monitoring the SINADS during its operation.

HM-4119

1280 X 1024 / 1024 X 768, 60Hz, 19" Non-Interlaced Color Display Monitor

The HM4119 is a 19" color monitor designed for CAD, CAM and CAE applications requiring an optimum price/performance relationship. Our latest 1280 x 1024/1024 x 768 non-interlaced monitor features newly developed technology like an EA (Elliptical Aperture) type lens for excellent focus and HSA (Hitachi Slit-winding with Auxiliary coil) yoke for 0.3/0.5 mm misconvergence. A convenient cabling layout is provided and an LSI video amplifier provides for a compact design.



Hitachi
Hitachi America, Ltd.
Office Automation Systems Division
East Coast Office: 59 Route 17 South, Allendale, New Jersey 07401, 201-825-8000
West Coast Office: 950 Elm Avenue, San Bruno, California 94066, 415-872-1902

HM4119

MONITOR PERFORMANCE AND SPECIFICATIONS

CRT size
20 inch (19V inch)
Electron gun
in line
Deflection angle
90°
Dot trio pitch
0.31mm
High contrast A/R coat
Optional

SIGNAL INPUT CHARACTERISTICS

Type
Analog RGB (composite sync on green)
Level
Composite: 1.0Vp-p (0.7-1.4 Vp-p)
Non composite: 0.7Vp-p (0.5-1.0Vp-p)
Signal polarity
Positive bright
Impedance—
terminated
75 ohms ± 2%
unterminated
Greater than 10K ohms

SYNC

Type
Comp. on green or external
Level
Composite: sync to total signal ratio=28.6 ± 5%
External: DC coupled TTL level
Signal polarity
Negative
Connectors
BNC for R, G, B and SYNC

ELECTRICAL PERFORMANCE

Resolution
1280 x 1024 [1024 x 768]
Scanning frequency
Horizontal: 61-65 kHz [48-52 kHz]
Vertical: 55-65 Hz
Retrace time
Horizontal: 3.5 μsec. max. [4.0 μsec. max]
Vertical: 550 μsec. max.

POWER REQUIREMENTS

Voltage
110V or 220V
Frequency
47-63 Hz
Consumption
Nominal: 140w/200VA
Maximum: 175w/250VA
Inrush current
Power on: less than 35 A
Manual degauss: less than 20 A

VIDEO

Bandwidth
100 MHz
Rise/fall time
5 nsec nominal [6 nsec nominal]
Overshoot
Less than 10% nominal of full scale
Sag
Less than 5% of full scale

DISPLAY

Active area
Horizontal: 360mm
Vertical 270mm
Convergence
0.3/0.5mm
Brightness
30 fl

USER CONTROLS

Brightness
Contrast
Degauss
Power on/off switch
Power on/off indicator

ENVIRONMENT

Temperature
Operating: 0-50°C (without cabinet)
Storage:−30-65°C
Humidity
Operating: 10-90% non-condensing
Storage: 10-90% non-condensing

Altitude
Operating: 10,000 feet
Shipping: 35,000 feet
Shock
10G
Vibration
0.5G

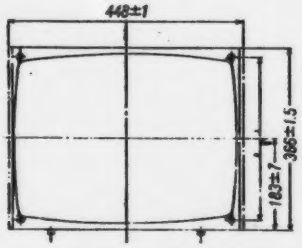
GENERAL

Weight
29 kg (without cabinet)
Size (w x h x d)
477.7 x 366 x 520mm (without cabinet)
Geometric distortion
Less than 1.5% of raster height
Raster size regulation
Horizontal: 1% max
Vertical: 1% max
Safety
Designed to meet UL478, CSA154 and VDE 0806
RF
FCC Class A

BASIC MODEL CONFIGURATION

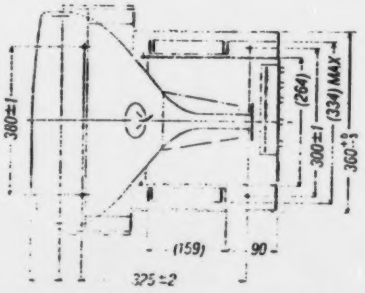
HM-4119-D-AA
61-65 kHz version, tilt and swivel cabinet Anti-glare panel (72% transmission)
HM-4119-D-AL
48-52 kHz version, tilt and swivel cabinet Anti-glare panel (72% transmission)

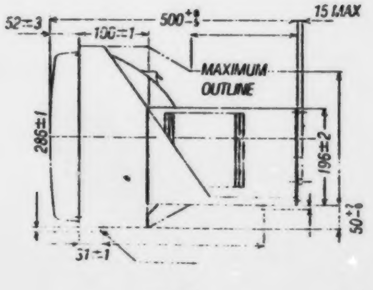
	ITEM	EQUATION	HM-4119-X-XA		HM-4119-X-XA		UNITS
			MONITOR REQUIREMENT	RECOMMENDED RATING	MONITOR REQUIREMENT	RECOMMENDED RATING	
a	Resolution H			1280		1024	Pixels
b	Resolution V			1024		768	Pixels
c	Pixel rate			9.3		15.88	ns
d	Pixel freq.	1/c		107.52		63.	MHz
e	H-DISP	axc		11.9		16.26	μs
f	H-BL	g+h+i	3.5-4.5	3.8	4.0-5.5	4.57	μs
g	H-FP		0.1-0.5	0.2	0.1-0.5	0.87	μs
h	H-SYNC		≥0.7	1.6	≥1.5	1.02	μs
i	H-BP		≥1.8	2.0	≥1.8	2.68	μs
j	1H	e+f		15.7		20.83	μs
k	H. freq.	1/j	61-65	63.7	48-52	48.0	KHz
l	V-DISP	bxj		(1024H)		(768H)	ms
m	V-BL	n+o+p		(37H)		(32H)	ms
n	V-FP		(>0H)	0	(>0H)	(1H)	ms
o	V-SYNC		(3H-6H)	(3H)	(2H-6H)	(3H)	ms
p	V-BP		(>33H)	(34H)	(≥27H)	(28H)	ms
q	1V	1+m		(1061H)		(800H)	ms
r	V. freq.	1/q	55-65	60.0	55-65	60.0 Hz	Hz



FRONT VIEW

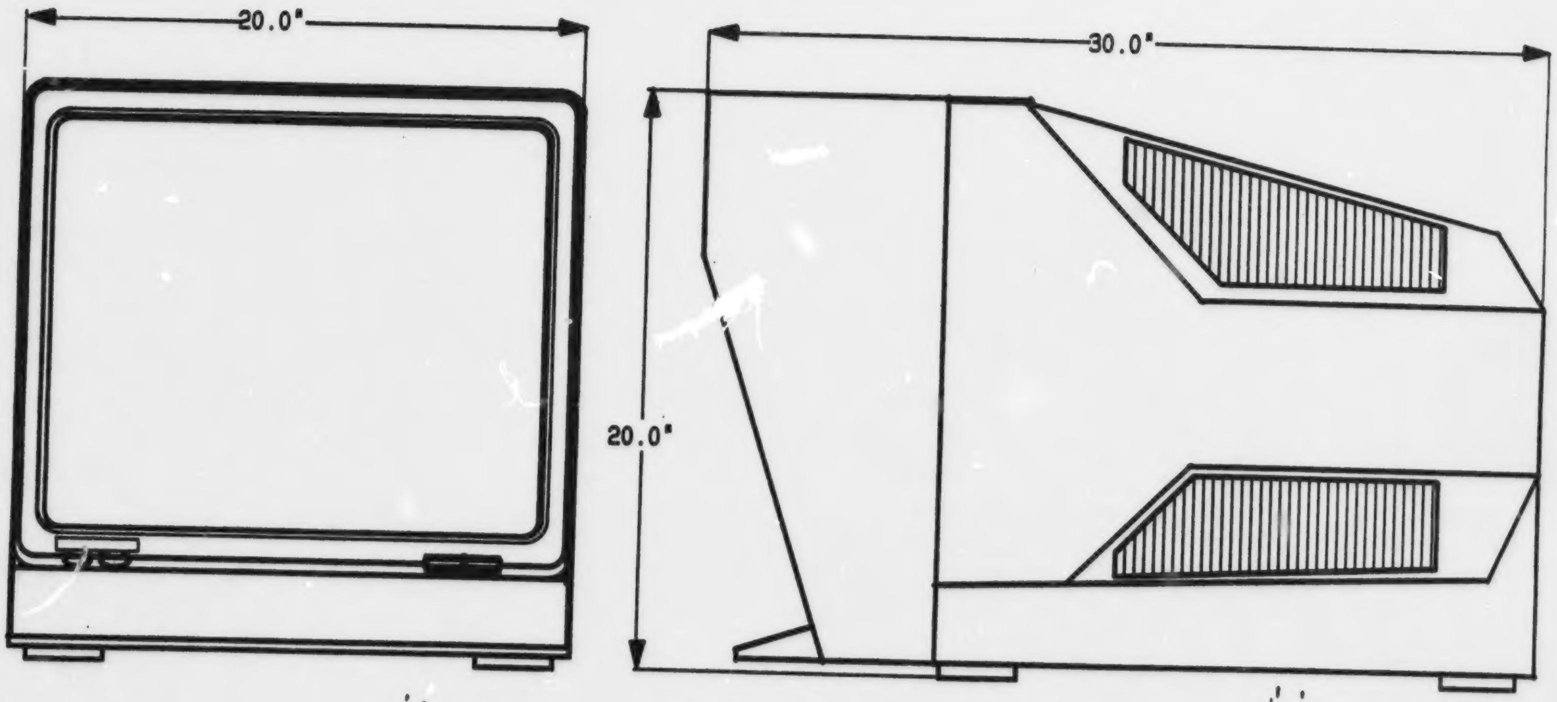
TOP VIEW





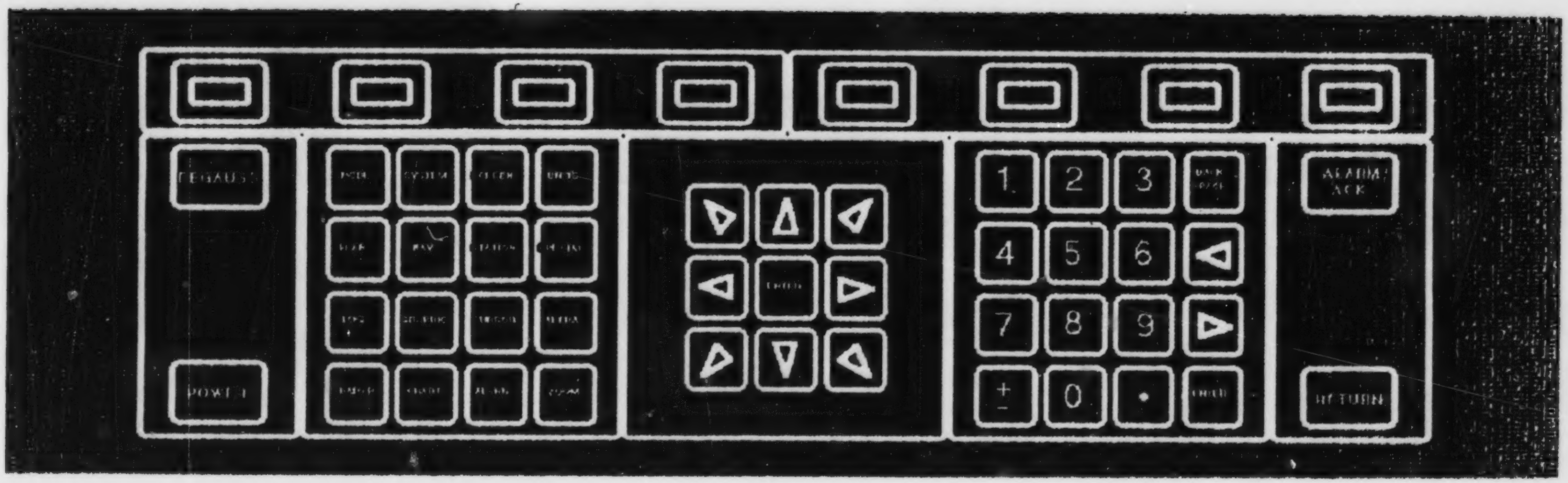
SIDE VIEW

DIMENSION: MM



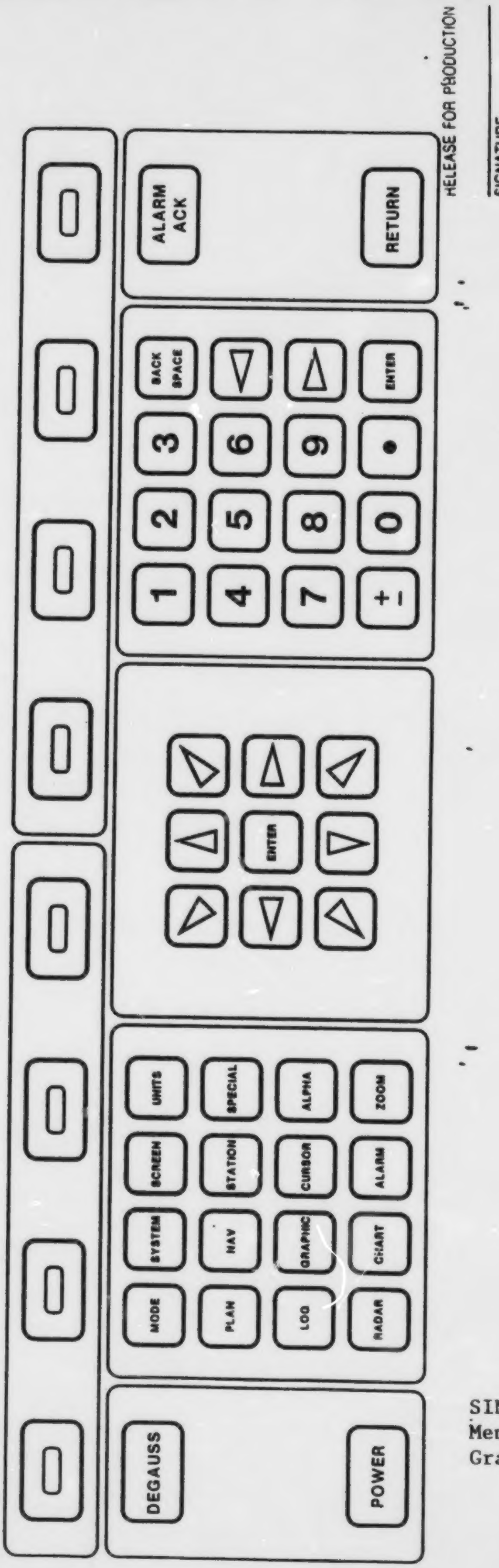
SINADS INTERACTIVE DISPLAY CONSOLE

Figure 4


DEGAUSS
SYSTEM
POWER
ENTER
1
2
3
BACK SPACE
4
5
6
7
8
9
±
0
•
ENTER
ALARM/ ACK
RETURN

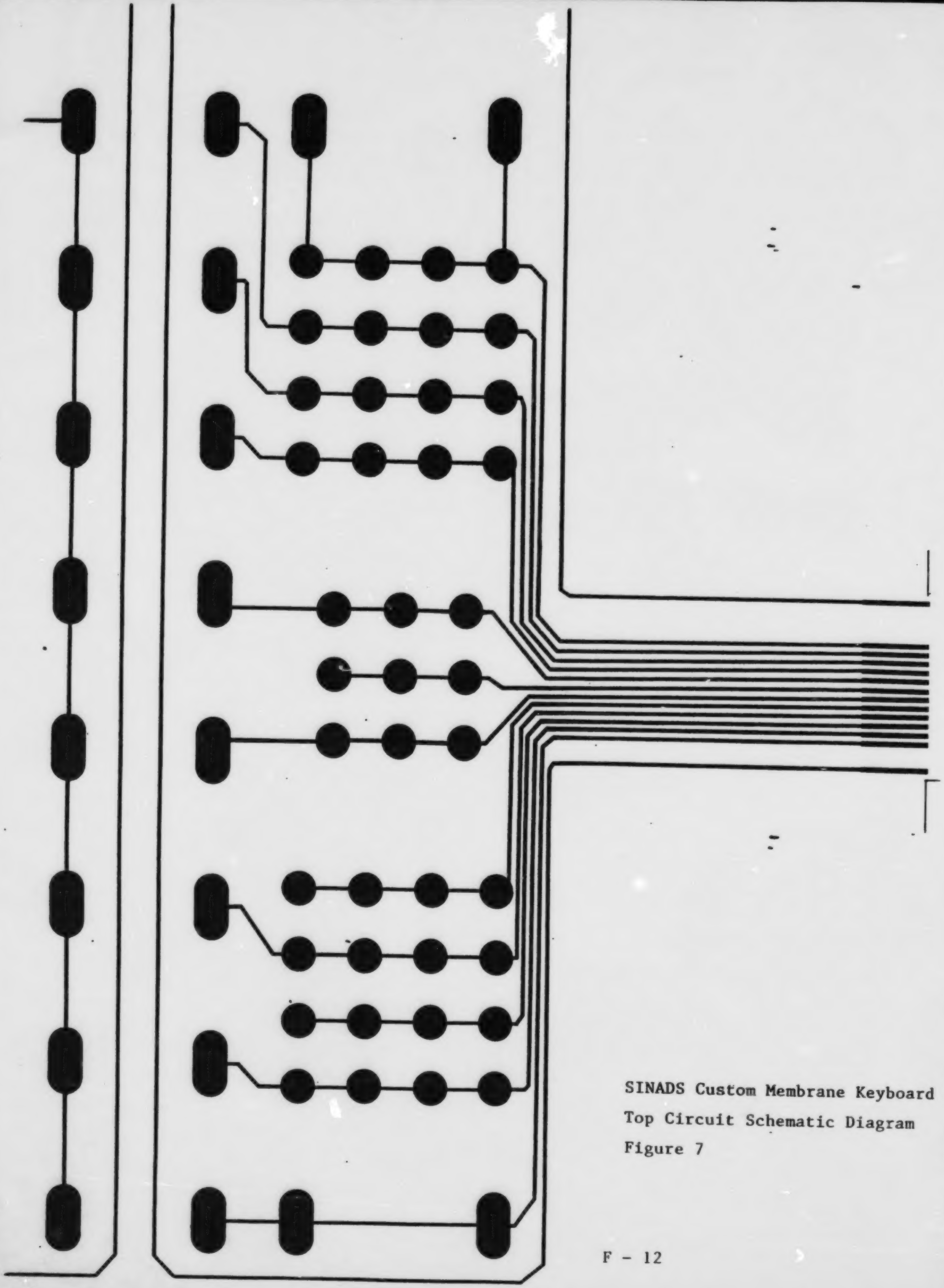
SINADS CUSTOM MEMBRANE KEYBOARD LAYOUT

Figure 5

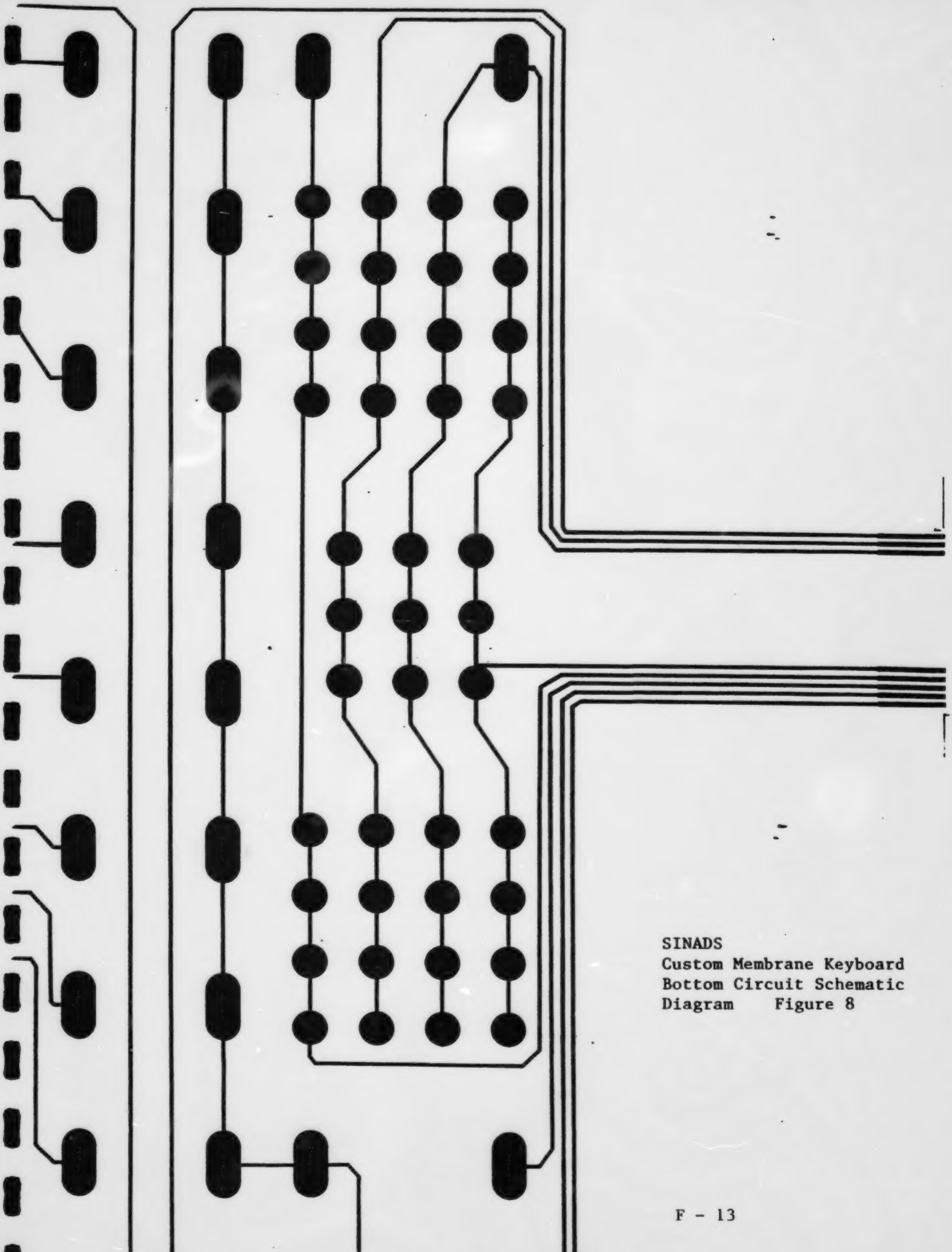

RELEASE FOR PRODUCTION
SIGNATURE
ALARM ACK
RETURN
BACK SPACE
ENTER
1
2
3
4
5
6
7
8
9
±
0
•
ENTER
MODE
SYSTEM
SCREEN
UNITS
PLAN
NAV
STATION
SPECIAL
LOG
GRAPHIC
CURSOR
ALPHA
RADAR
CHART
ALARM
ZOOM
DEGAUSS
POWER

SINADS Custom
Membrane Keyboard
Graphics Layout

Figure 6



SINADS Custom Membrane Keyboard
Top Circuit Schematic Diagram
Figure 7



SINADS
Custom Membrane Keyboard
Bottom Circuit Schematic
Diagram Figure 8

Multifunction Osl KEYboard Controller V1.0
Programming Manual

Overview

The keyboard controller has the following capabilities:

i) encode an 8 * 12 keyboard matrix into printable ascii characters.
ii) store and execute ROMed or downloaded sound macros
iii) keyboard or host computer control of power and degauss switches
iv) programmable key debounce time
v) ROM and RAM memory self test

Serial Interface Specifications

- RS232-C asynchronous serial interface
- 9600 baud
- 8 bits/character
- 1 start bit
- 1 stop bit
- no parity
- xon/xoff control of host computers transmissions
  i.e. the controller will not respond to xon/xoff from the host

Commands

All numeric paramaters following commands must be the ascii representatio of the hex digit. All commands must be terminated by the command terminator 'CR', ascii carriage return. The controller will respond to any command sequence errors with a ascii 'NAK' after the 'CR' command terminator. If an error is detected command execution is aborted.

'X' command
- execute ROM stored sound macro

format X[number]'CR'
where: number = macro number, range 0 -> F

e.g. to execute sound macro number 10 from ROM
XA'CR'

'U' command
- execute RAM stored sound macro

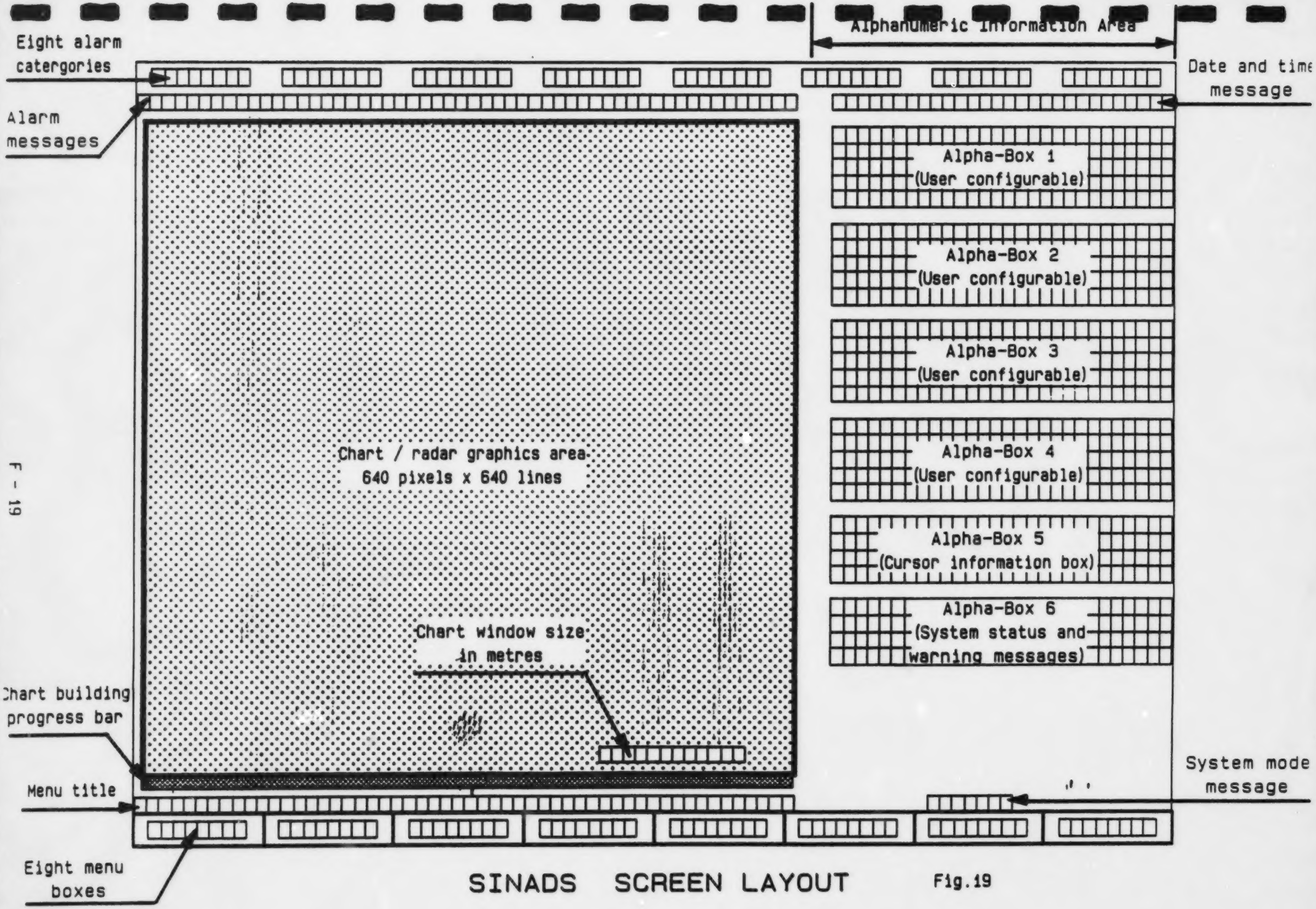
format U[number]'CR'
where: number = macro number, range 0 -> F

e.g. to execute sound macro number 3 from RAM
U3'CR'

'S' command
- store sound macro in RAM

```
        - each sound macro is composed of a series of one or more tone
          sequences, each tone sequence is composed of 3 bytes(6 asc. digits)
          a maximum of 85 tone sequences may make up any one sound macro.

        format S[number][attenuation][tone nibble 1][t.n. 2][t.n. 3][duration
               nibble 1][d.n. 2]....  .'CR'

            where: number = macro number, range 0 -> F
                   attenuation = attenuation in 2db increments, range 1 -> F
                                 (i.e. 2db -> 30 db)
                                 note: a '0' in the attenuation nibble is an
                                       error.
                   tone nibbles 1->3 = tone frequency, the tone frequency
                                       is a 10 bit number and is calculated
                                       using the following formula:
                                          n = 125,000/frequency(Hz)
                                       valid range 000 -> 3FF
                   duration nibbles 1,2 = the duration of the tone in 33 ms
                                          increments, valid range 00 -> FF

        e.g. to store macro #3 which consists of a 1 Kz tone at -2 db for
            1 second and a 12.5 Kz tone at -10 db for 0.5 seconds.

            macro #3 = 3
            -2 db = 1
            1 Kz = 07D
            1 second = 1E
            -10 db = 5
            12.5 Kz = 00A
            0.5 seconds = 0F

            therefore input the string  S3107D1E500A0F'CR'

    'P' command
        - power switch on/off command
        - power on will cause a 'ping' sound  macro to execute
        - when the power switch is off the keyboard is disabled

        format P[on/off bit]'CR'
            where on/off bit = 0(off) or 1(on)

        e.g. turn power switch on
            P1'CR'


    'G' command
        - degauss switch on/off command

        format G[on/off bit]'CR'
            where on/off bit = 0(off) or 1(on)

        e.g. turn degauss switch off
            G0'CR'

    'T' command
        - set key debounce time (default = 70 milliseconds)
```

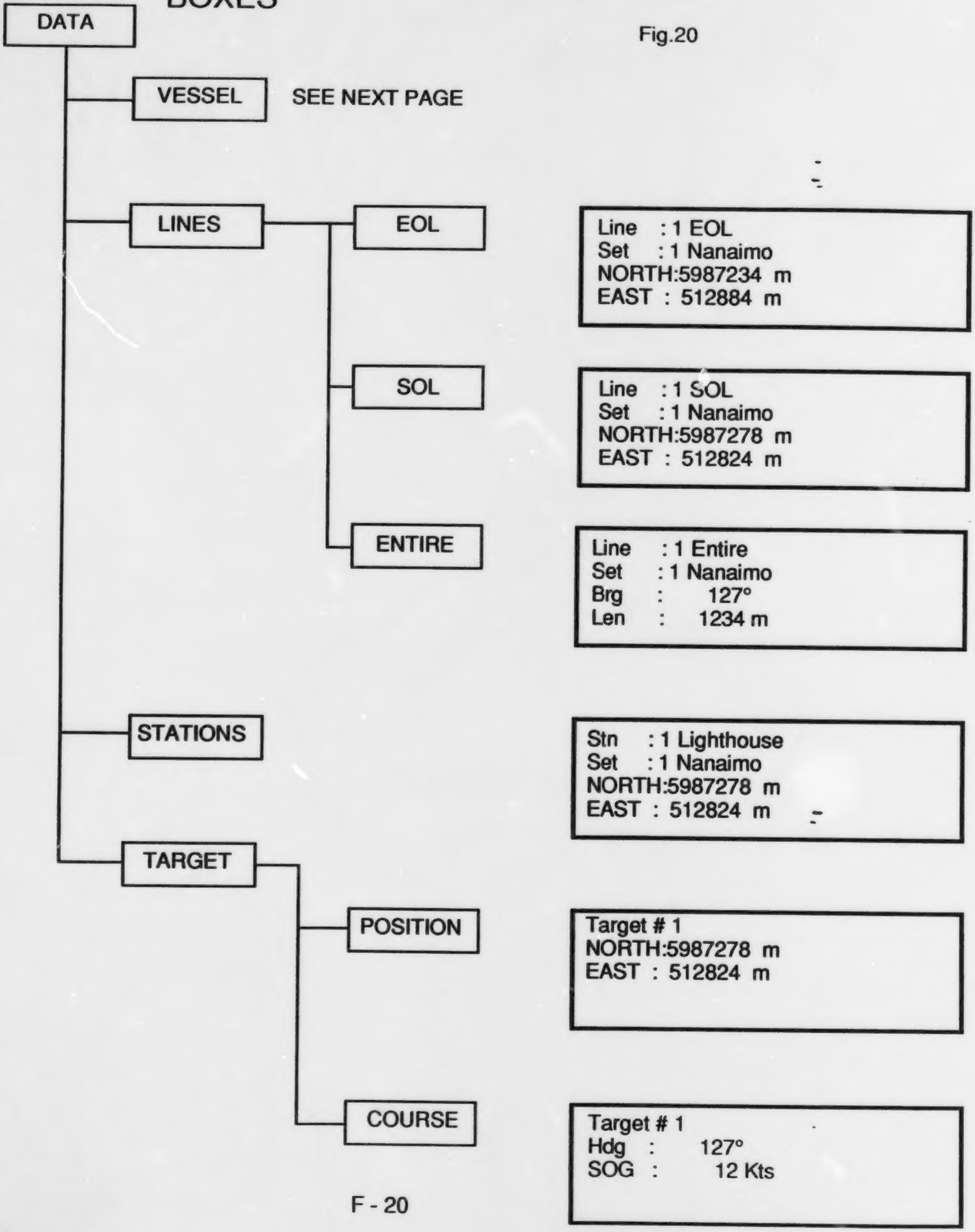
```
          format T[time high nibble][time low nibble]'CR'
               where time nibbles 1 and 2 = time byte in 10 ms increments,
                                              valid range 00 -> FF

          e.g. to set debounce time to 100 milliseconds
               T64'CR'

     'M' command
          - RAM and ROM self test
          - the RAM test is a walk a bit test on every memory location
          - the ROM test is a 16 bit checksum test

          format M'CR'

     'Break' command
          - equivalent to a restart or reset command
          - note: disconnecting the serial cable will cause a 'Break'
          - on 'Break' the controller will output an initialization string

Power up Sequence

     - on power up the controller will output a string indicating the
       firmware version number, currently the string is:
          crlfcrlfMONKEY C V1.0crlfcrlf
       also, a 'ping' sound macro is generated, the power switch assumes
       an 'on' position and the degauss switch assumes an 'off' position

EPROM Programming

     - once a sound macro has been composed by downloading to RAM it may
       be permanently stored in ROM, the macro number multiplied by
       100 hex is the beginning address of the macro e.g. macro A must
       be stored beginning at address A00 hex. The macro must be terminated
       by a byte whose value is 00 hex. Unused macros should have a 00 byte
       at their beginning address. Once the EPROM has been programmed a 16
       bit checksum must be calculated, most EPROM programmers will do this
       for you. The last two bytes of the EPROM must be reprogrammed with
       the 16 bit checksum value i.e. location FFE is programmed with the
       high byte of the checksum and location FFE is programmed with the
       low byte of the checksum.

Key Matrix Encoding

     - the following table is the ascii encoding map for the keyboard matrix


          C1R1      FCB       20H                 COLUMN 1  ROW 1 -> ASCII 'SPACE'
          C1R2      FCB       21H                 COLUMN 1  ROW 2 -> ASCII '!'
          C1R3      FCB       22H                 COLUMN 1  ROW 3 -> ASCII '"'
          C1R4      FCB       23H                 COLUMN 1  ROW 4 -> ASCII '#'
          C1R5      FCB       24H                 COLUMN 1  ROW 5 -> ASCII '$'
          C1R6      FCB       25H                 COLUMN 1  ROW 6 -> ASCII '%'
          C1R7      FCB       26H                 COLUMN 1  ROW 7 -> ASCII '&'
          C1R8      FCB       27H                 COLUMN 1  ROW 8 -> ASCII '''
          C1R9      FCB       28H                 COLUMN 1  ROW 9 -> ASCII '('
        C1R10   FCB     29H             COLUMN 1  ROW 10-> ASCII ')'
        C1R11   FCB     2AH             COLUMN 1  ROW 11-> ASCII '*'
        C1R12   FCB     2BH             COLUMN 1  ROW 12-> ASCII '+'
        C2R1    FCB     2CH             COLUMN 2  ROW 1 -> ASCII ','
        C2R2    FCB     2DH             COLUMN 2  ROW 2 -> ASCII '-'
        C2R3    FCB     2EH             COLUMN 2  ROW 3 -> ASCII '.'
        C2R4    FCB     2FH             COLUMN 2  ROW 4 -> ASCII '/'
        C2R5    FCB     30H             COLUMN 2  ROW 5 -> ASCII '0'
        C2R6    FCB     31H             COLUMN 2  ROW 6 -> ASCII '1'
        C2R7    FCB     32H             COLUMN 2  ROW 7 -> ASCII '2'
        C2R8    FCB     33H             COLUMN 2  ROW 8 -> ASCII '3'
        C2R9    FCB     34H             COLUMN 2  ROW 9 -> ASCII '4'
        C2R10   FCB     35H             COLUMN 2  ROW 10-> ASCII '5'
        C2R11   FCB     36H             COLUMN 2  ROW 11-> ASCII '6'
        C2R12   FCB     37H             COLUMN 2  ROW 12-> ASCII '7'
        C3R1    FCB     38H             COLUMN 3  ROW 1 -> ASCII '8'
        C3R2    FCB     39H             COLUMN 3  ROW 2 -> ASCII '9'
        C3R3    FCB     3AH             COLUMN 3  ROW 3 -> ASCII ':'
        C3R4    FCB     3BH             COLUMN 3  ROW 4 -> ASCII ';'
        C3R5    FCB     3CH             COLUMN 3  ROW 5 -> ASCII '<'
        C3R6    FCB     3DH             COLUMN 3  ROW 6 -> ASCII '='
        C3R7    FCB     3EH             COLUMN 3  ROW 7 -> ASCII '>'
        C3R8    FCB     3FH             COLUMN 3  ROW 8 -> ASCII '?'
        C3R8    FCB     40H             COLUMN 3  ROW 9 -> ASCII '@'
        C3R10   FCB     41H             COLUMN 3  ROW 10-> ASCII 'A'
        C3R11   FCB     42H             COLUMN 3  ROW 11-> ASCII 'B'
        C3R12   FCB     43H             COLUMN 3  ROW 12-> ASCII 'C'
        C4R1    FCB     44H             COLUMN 4  ROW 1 -> ASCII 'D'
        C4R2    FCB     45H             COLUMN 4  ROW 2 -> ASCII 'E'
        C4R3    FCB     46H             COLUMN 4  ROW 3 -> ASCII 'F'
        C4R4    FCB     47H             COLUMN 4  ROW 4 -> ASCII 'G'
        C4R5    FCB     48H             COLUMN 4  ROW 5 -> ASCII 'H'
        C4R6    FCB     49H             COLUMN 4  ROW 6 -> ASCII 'I'
        C4R7    FCB     4AH             COLUMN 4  ROW 7 -> ASCII 'J'
        C4R8    FCB     4BH             COLUMN 4  ROW 8 -> ASCII 'K'
        C4R9    FCB     4CH             COLUMN 4  ROW 9 -> ASCII 'L'
        C4R10   FCB     4DH             COLUMN 4  ROW 10-> ASCII 'M'
        C4R11   FCB     4EH             COLUMN 4  ROW 11-> ASCII 'N'
        C4R12   FCB     4FH             COLUMN 4  ROW 12-> ASCII 'O'
        C5R1    FCB     50H             COLUMN 5  ROW 1 -> ASCII 'P'
        C5R2    FCB     51H             COLUMN 5  ROW 2 -> ASCII 'Q'
        C5R3    FCB     52H             COLUMN 5  ROW 3 -> ASCII 'R'
        C5R4    FCB     53H             COLUMN 5  ROW 4 -> ASCII 'S'
        C5R5    FCB     54H             COLUMN 5  ROW 5 -> ASCII 'T'
        C5R6    FCB     55H             COLUMN 5  ROW 6 -> ASCII 'U'
        C5R7    FCB     56H             COLUMN 5  ROW 7 -> ASCII 'V'
        C5R8    FCB     57H             COLUMN 5  ROW 8 -> ASCII 'W'
        C5R9    FCB     58H             COLUMN 5  ROW 9 -> ASCII 'X'
        C5R10   FCB     59H             COLUMN 5  ROW 10-> ASCII 'Y'
        C5R11   FCB     5AH             COLUMN 5  ROW 11-> ASCII 'Z'
        C5R12   FCB     5BH             COLUMN 5  ROW 12-> ASCII '['
        C6R1    FCB     5CH             COLUMN 6  ROW 1 -> ASCII '\'
        C6R2    FCB     5DH             COLUMN 6  ROW 2 -> ASCII ']'
        C6R3    FCB     5EH             COLUMN 6  ROW 3 -> ASCII 'carat'
        C6R4    FCB     5FH             COLUMN 6  ROW 4 -> ASCII '_'
        C6R5    FCB     60H             COLUMN 6  ROW 5 -> ASCII '`'
        C6R6    FCB     61H             COLUMN 6  ROW 6 -> ASCII 'a'
        C6R7    FCB     62H             COLUMN 6  ROW 7 -> ASCII 'b'
        C6R8    FCB     63H             COLUMN 6  ROW 8 -> ASCII 'c'
        C6R9    FCB     64H             COLUMN 6  ROW 9 -> ASCII 'd'
        C6R10   FCB     65H             COLUMN 6  ROW 10-> ASCII 'e'
        C6R11   FCB     66H             COLUMN 6  ROW 11-> ASCII 'f'
        C6R12   FCB     67H             COLUMN 6  ROW 12-> ASCII 'g'
        C7R1    FCB     68H             COLUMN 7  ROW 1 -> ASCII 'h'
        C7R2    FCB     69H             COLUMN 7  ROW 2 -> ASCII 'i'
        C7R3    FCB     6AH             COLUMN 7  ROW 3 -> ASCII 'j'
        C7R4    FCB     6BH             COLUMN 7  ROW 4 -> ASCII 'k'
        C7R5    FCB     6CH             COLUMN 7  ROW 5 -> ASCII 'l'
        C7R6    FCB     6DH             COLUMN 7  ROW 6 -> ASCII 'm'
        C7R7    FCB     6EH             COLUMN 7  ROW 7 -> ASCII 'n'
        C7R8    FCB     6FH             COLUMN 7  ROW 8 -> ASCII 'o'
        C7R9    FCB     70H             COLUMN 7  ROW 9 -> ASCII 'p'
        C7R10   FCB     71H             COLUMN 7  ROW 10-> ASCII 'q'
        C7R11   FCB     72H             COLUMN 7  ROW 11-> ASCII 'r'
        C7R12   FCB     73H             COLUMN 7  ROW 12-> ASCII 's'
        C8R1    FCB     74H             COLUMN 8  ROW 1 -> ASCII 't'
        C8R2    FCB     75H             COLUMN 8  ROW 2 -> ASCII 'u'
        C8R3    FCB     76H             COLUMN 8  ROW 3 -> ASCII 'v'
        C8R4    FCB     77H             COLUMN 8  ROW 4 -> ASCII 'w'
        C8R5    FCB     78H             COLUMN 8  ROW 5 -> ASCII 'x'
        C8R6    FCB     79H             COLUMN 8  ROW 6 -> ASCII 'y'
        C8R7    FCB     7AH             COLUMN 8  ROW 7 -> ASCII 'z'
        C8R8    FCB     7BH             COLUMN 8  ROW 8 -> ASCII '{'
        C8R9    FCB     7CH             COLUMN 8  ROW 9 -> ASCII '|'
        C8R10   FCB     7DH             COLUMN 8  ROW 10-> ASCII '}'
        C8R11   FCB     7EH             COLUMN 8  ROW 11-> ASCII 'tilde'
        C8R12   FCB     7FH             COLUMN 8  ROW 12-> ASCII 'DEL'
```


Alphanumeric Information Area
Eight alarm catergories
Alarm messages
Date and time message
Alpha-Box 1 (User configurable)
Alpha-Box 2 (User configurable)
Alpha-Box 3 (User configurable)
Alpha-Box 4 (User configurable)
Alpha-Box 5 (Cursor information box)
Alpha-Box 6 (System status and warning messages)
Chart / radar graphics area
640 pixels x 640 lines
Chart window size in metres
Chart building progress bar
Menu title
System mode message
Eight menu boxes

SINADS SCREEN LAYOUT Fig.19

EXAMPLES OF CONTENT OF SINADS ALPHA BOXES

Fig.20


DATA
VESSEL
SEE NEXT PAGE
LINES
EOL
SOL
ENTIRE
STATIONS
TARGET
POSITION
COURSE

Line : 1 EOL
Set : 1 Nanaimo
NORTH:5987234 m
EAST : 512884 m

Line : 1 SOL
Set : 1 Nanaimo
NORTH:5987278 m
EAST : 512824 m

Line : 1 Entire
Set : 1 Nanaimo
Brg : 127°
Len : 1234 m

Stn : 1 Lighthouse
Set : 1 Nanaimo
NORTH:5987278 m
EAST : 512824 m

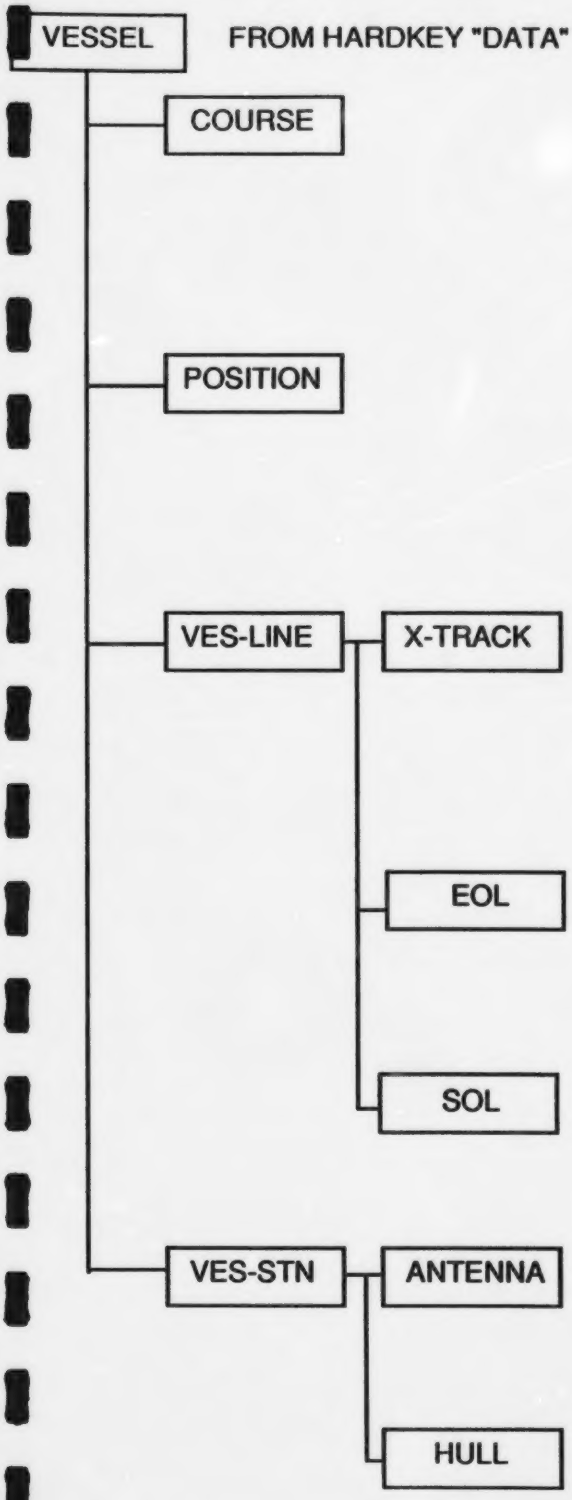
Target # 1
NORTH:5987278 m
EAST : 512824 m

Target # 1
Hdg : 127°
SOG : 12 Kts

EXAMPLES OF CONTENT OF SINADS ALPHA BOXES

FROM HARDKEY "DATA"

Fig.20


VESSEL
COURSE
POSITION
VES-LINE
X-TRACK
EOL
SOL
VES-STN
ANTENNA
HULL

GYRO : 270°
CMG : 271°
SPD : 12 Kts
SOG : 12 Kts

Vessel
NORTH:5960000 m
EAST : 545210 m
FQ : 4 m

Ves-Line : 1 - Xtrack
Line Set : 1 Nanaimo
Dist : 50 m

Ves-Line : 1 - EOL
Line Set : 1 Nanaimo
RNG : 1234 m
BRG : 12°

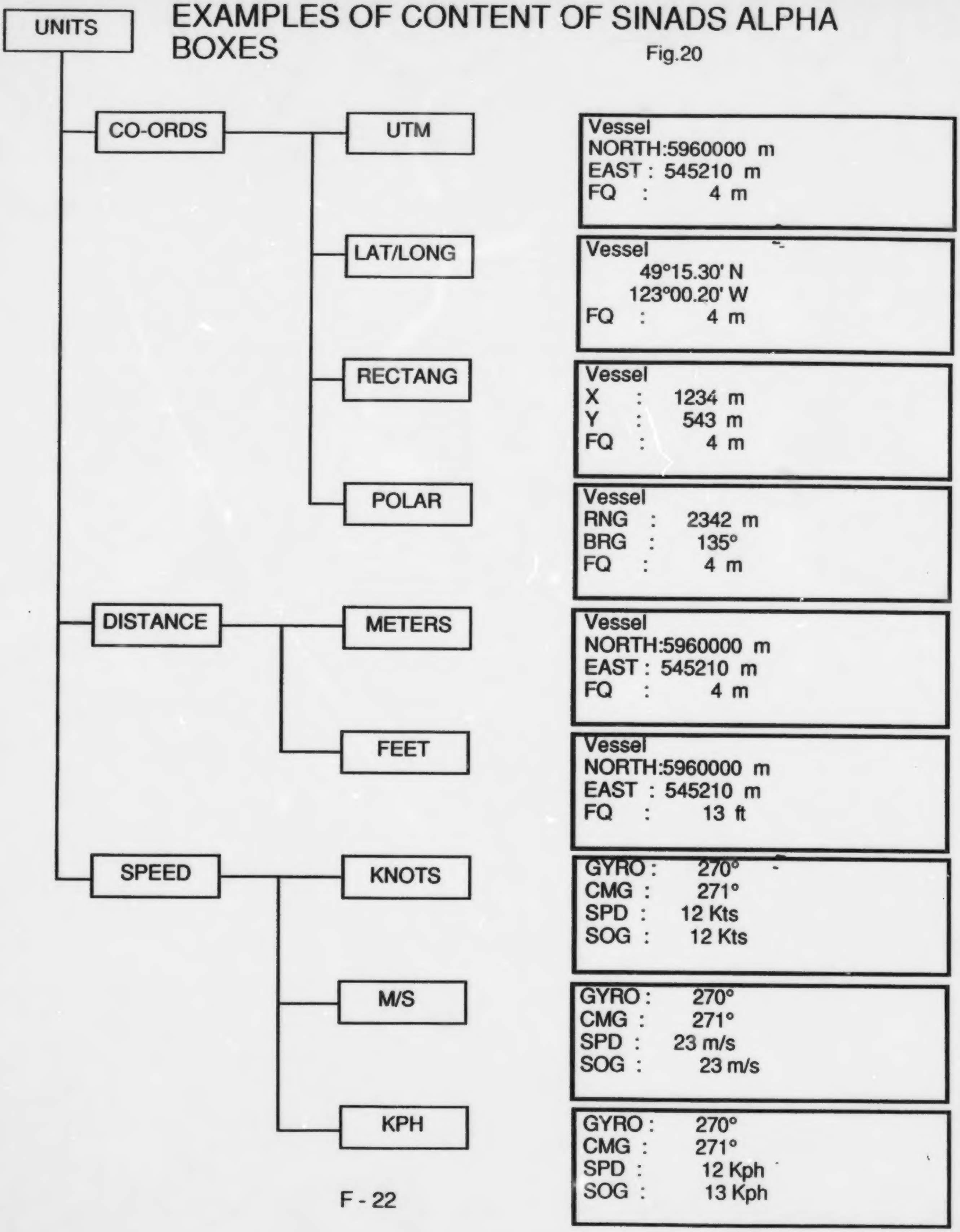
Ves-Line : 1 - SOL
Line Set : 1 Nanaimo
RNG : 103 m
BRG : 2°

Antenna-Stn : 1 Lthouse
Stn Set : 1 Microwav
RNG : 303 m
BRG : 45°

Hull-Stn : 1 Lthouse
Stn Set : 1 Microwav
RNG : 303 m
BRG : 45°

EXAMPLES OF CONTENT OF SINADS ALPHA BOXES

Fig.20


UNITS
CO-ORDS
UTM
LAT/LONG
RECTANG
POLAR
DISTANCE
METERS
FEET
SPEED
KNOTS
M/S
KPH

Vessel
NORTH:5960000 m
EAST : 545210 m
FQ : 4 m

Vessel
49°15.30' N
123°00.20' W
FQ : 4 m

Vessel
X : 1234 m
Y : 543 m
FQ : 4 m

Vessel
RNG : 2342 m
BRG : 135°
FQ : 4 m

Vessel
NORTH:5960000 m
EAST : 545210 m
FQ : 4 m

Vessel
NORTH:5960000 m
EAST : 545210 m
FQ : 13 ft

GYRO : 270°
CMG : 271°
SPD : 12 Kts
SOG : 12 Kts

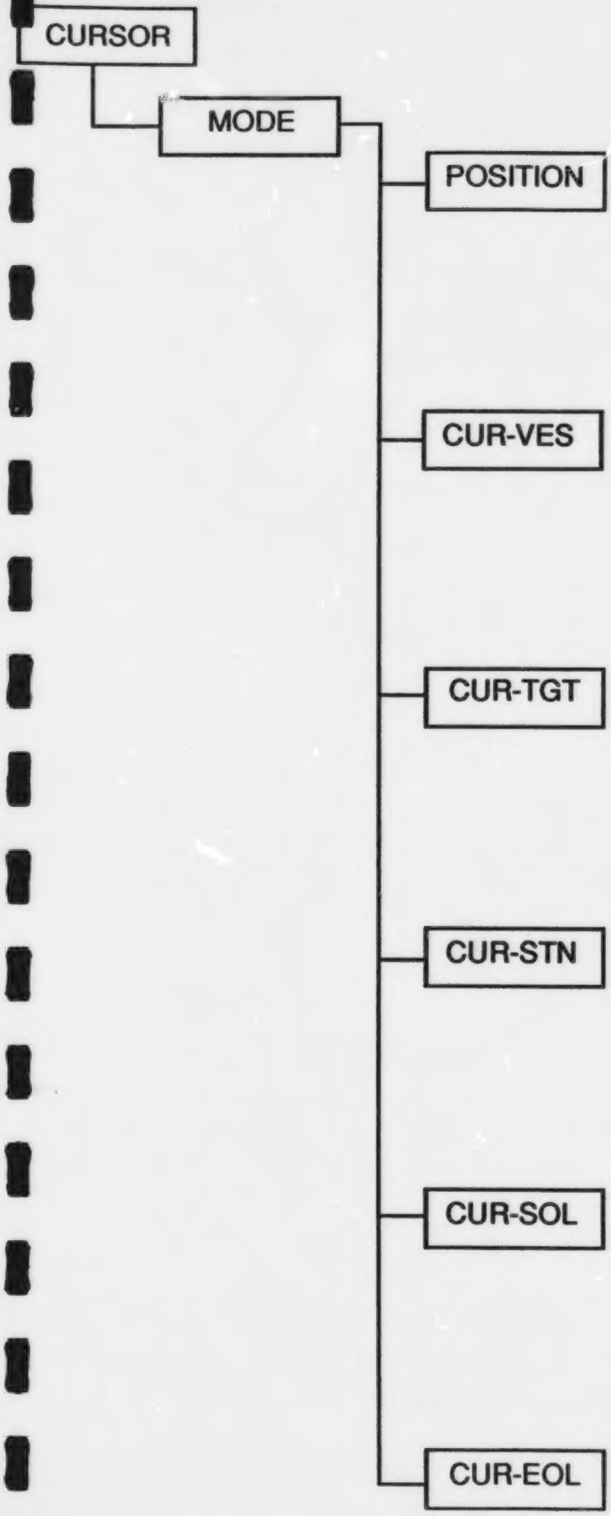
GYRO : 270°
CMG : 271°
SPD : 23 m/s
SOG : 23 m/s

GYRO : 270°
CMG : 271°
SPD : 12 Kph
SOG : 13 Kph

EXAMPLES OF CONTENT OF SINADS ALPHA BOXES

URSOR DISPLAYS

Fig.20


CURSOR
MODE
POSITION
CUR-VES
CUR-TGT
CUR-STN
CUR-SOL
CUR-EOL

```
Cursor
NORTH:5960000  m
EAST  : 545210  m
```

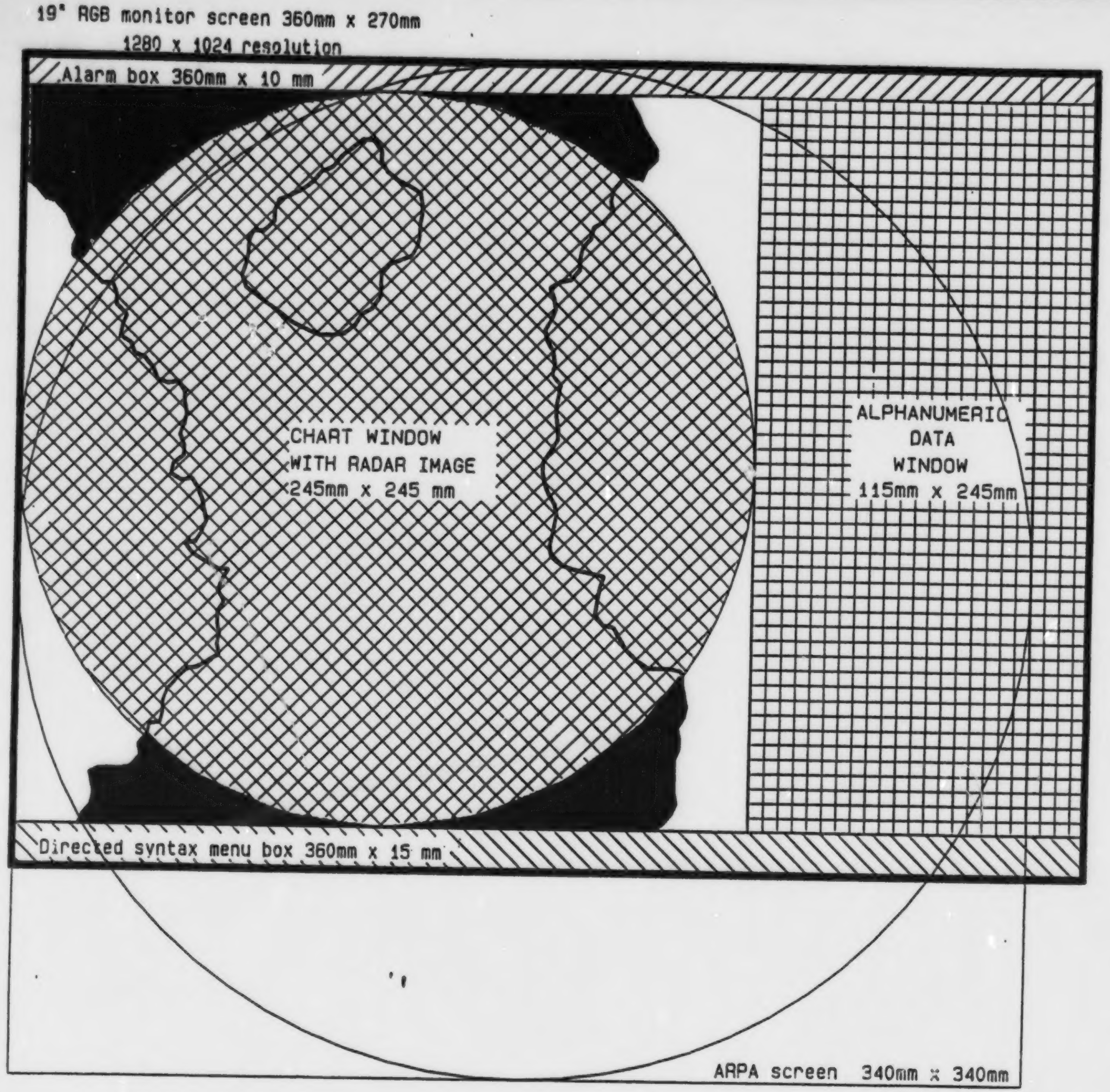
```
Vessel to Cursor
RNG   :     2342  m
BRG   :      135°
```

```
Target to Cursor-#1
RNG   :     2342  m
BRG   :      135°
```

```
Stn to Cursor-#1 : Lthouse
Stn Set #1 : Microwav
RNG   :     2342  m
BRG   :      135°
```

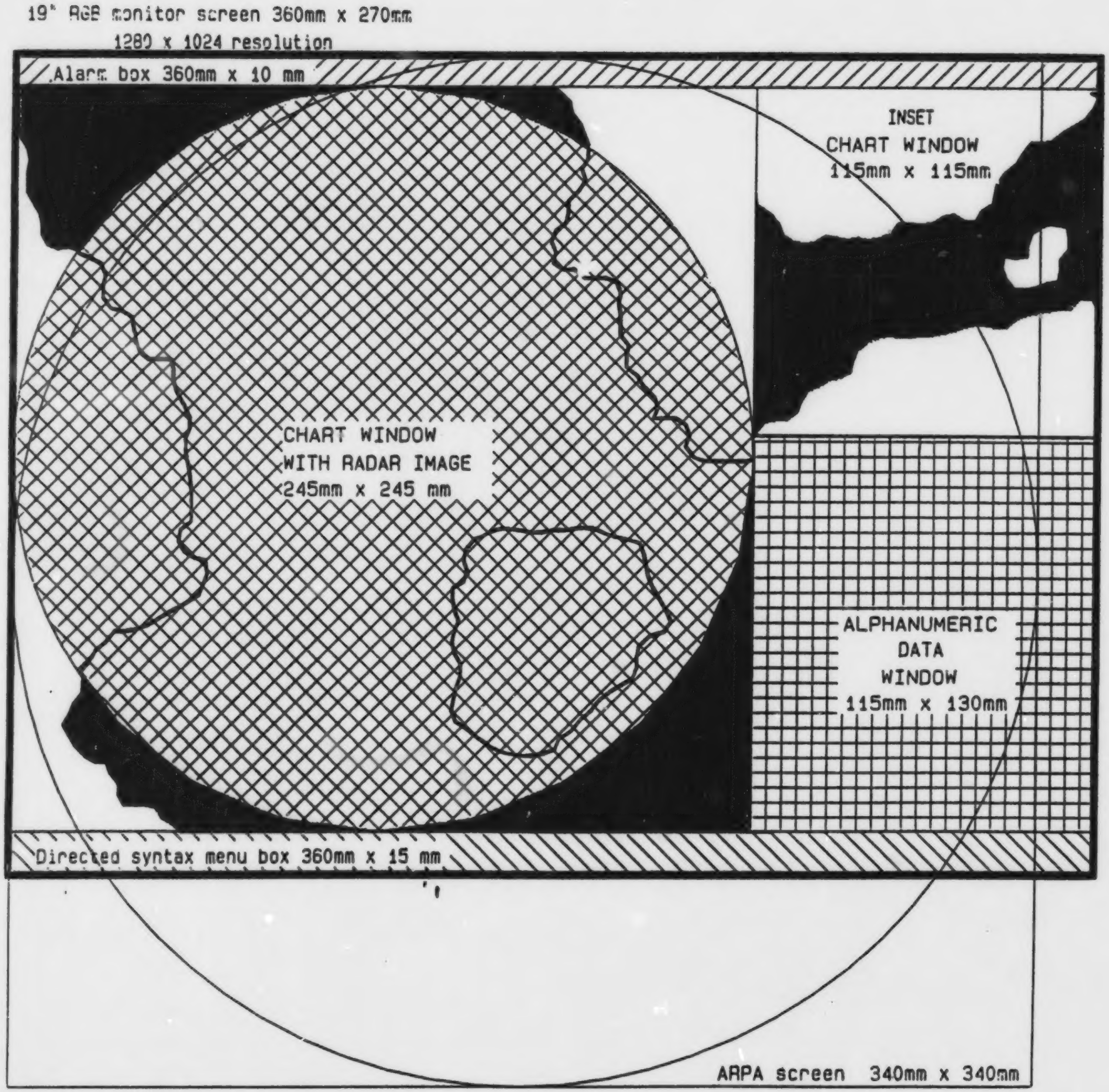
```
Line to Cursor-#1-SOL
Line Set #1 : Nanaimo
RNG   :     2342  m
BRG   :      135°
```

```
Line to Cursor-#1-EOL
Line Set #1 : Nanaimo
RNG   :     1348  m
BRG   :      120°
```


19" RGB monitor screen 360mm x 270mm
1280 x 1024 resolution
Alarm box 360mm x 10 mm
CHART WINDOW
WITH RADAR IMAGE
245mm x 245 mm
ALPHANUMERIC
DATA
WINDOW
115mm x 245mm
Directed syntax menu box 360mm x 15 mm
ARPA screen 340mm x 340mm

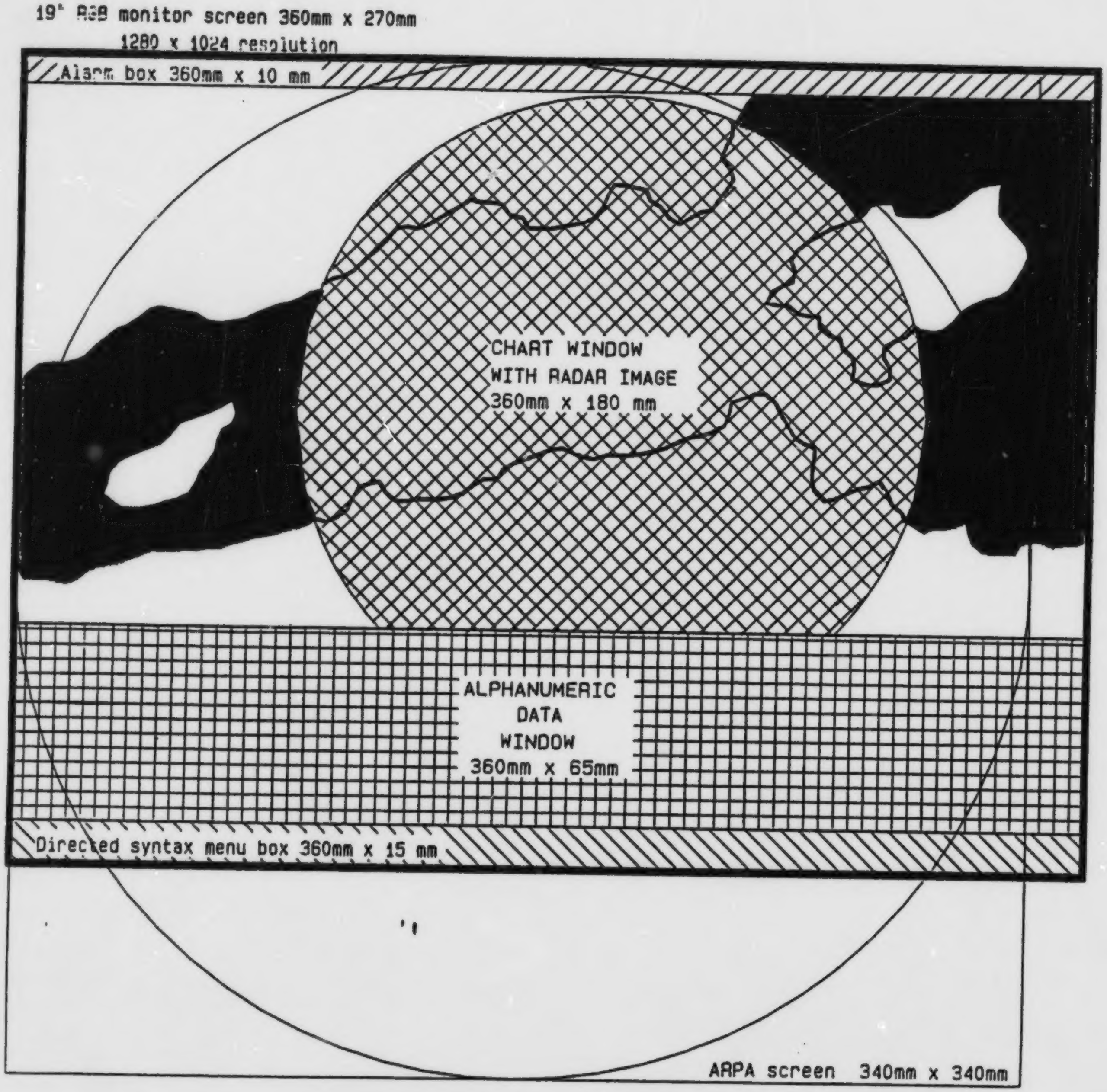
SINADS
SINGLE CHART
PRESENTATION
WITH SIDE
ALPHA

Fig. 14


19" RGB monitor screen 360mm x 270mm
1280 x 1024 resolution
Alarm box 360mm x 10 mm
INSET
CHART WINDOW
115mm x 115mm
CHART WINDOW
WITH RADAR IMAGE
245mm x 245 mm
ALPHANUMERIC
DATA
WINDOW
115mm x 130mm
Directed syntax menu box 360mm x 15 mm
ARPA screen 340mm x 340mm

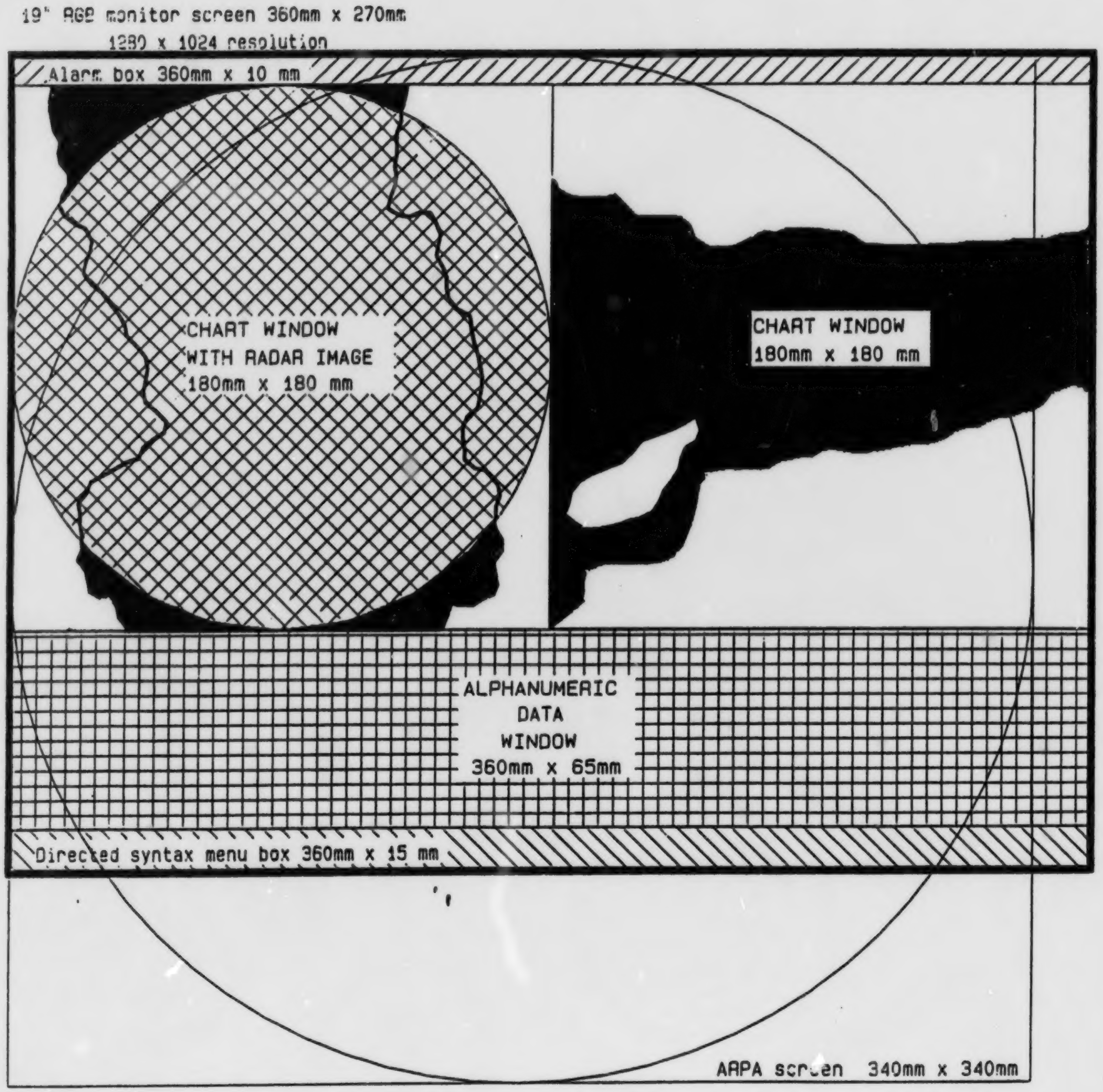
SINADS
SINGLE CHART
WITH INSET
PRESENTATION

Figure 15


19" RGB monitor screen 360mm x 270mm
1280 x 1024 resolution
Alarm box 360mm x 10 mm
CHART WINDOW
WITH RADAR IMAGE
360mm x 180 mm
ALPHANUMERIC
DATA
WINDOW
360mm x 65mm
Directed syntax menu box 360mm x 15 mm
ARPA screen 340mm x 340mm

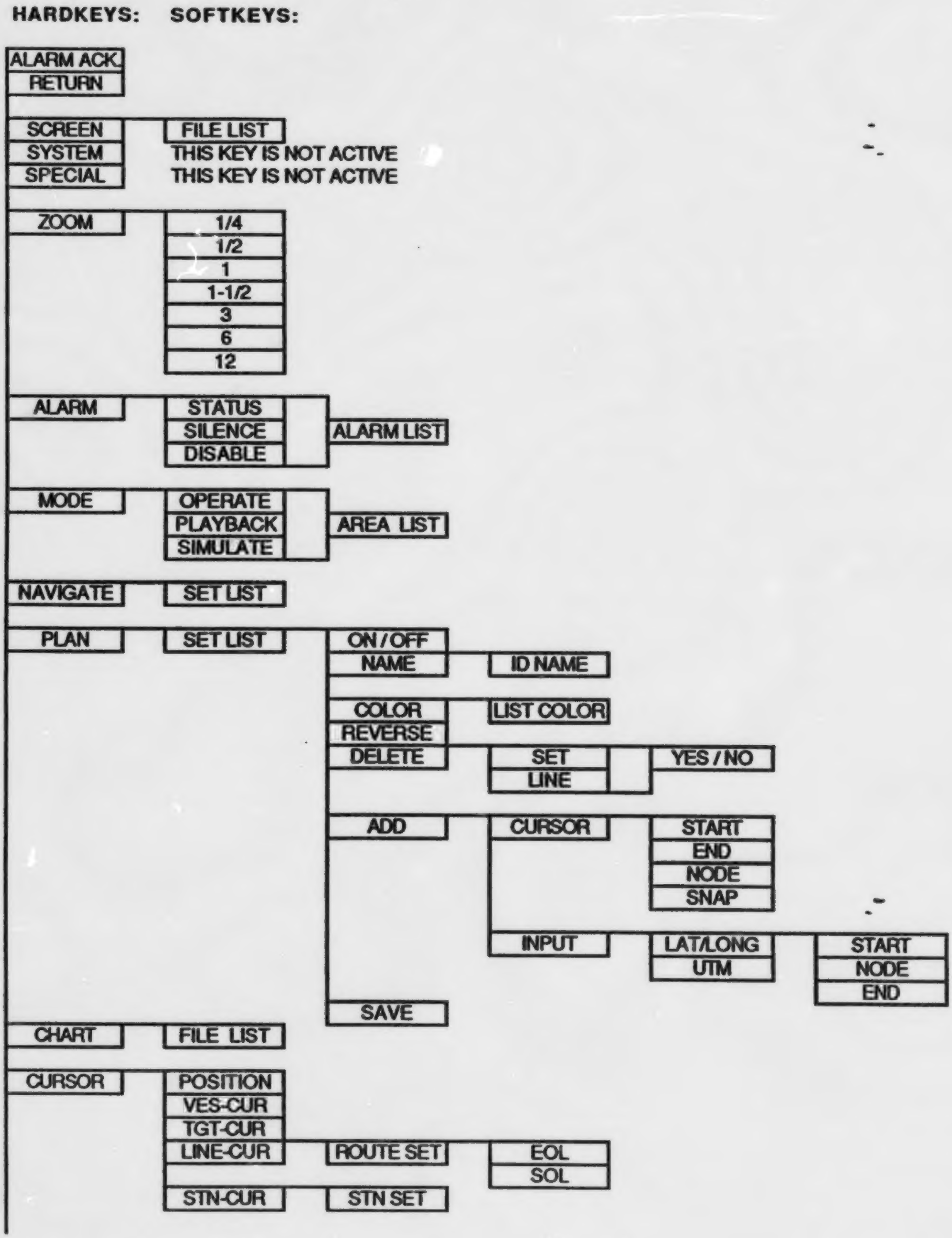
SINADS
SINGLE CHART
PRESENTATION
WITH LOWER
ALPHA

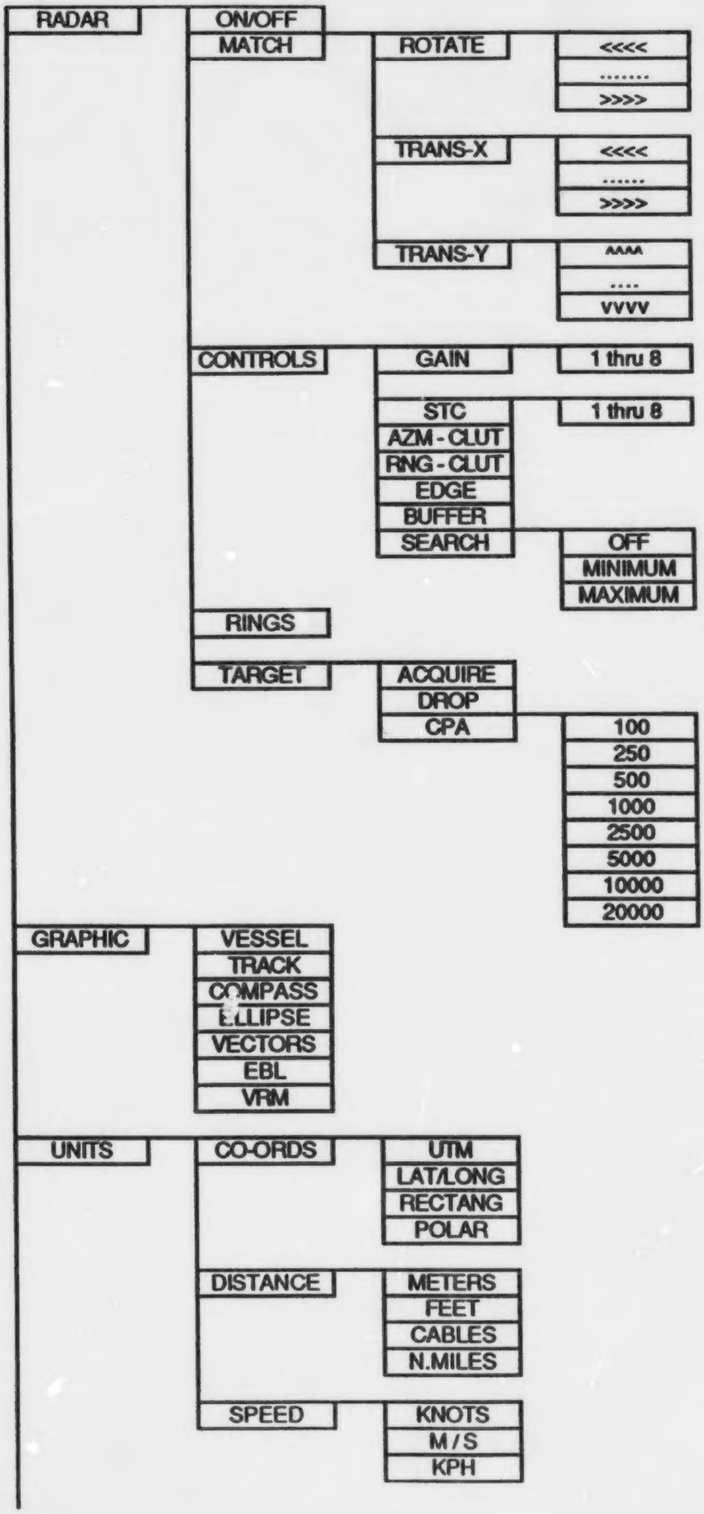
Figure 16

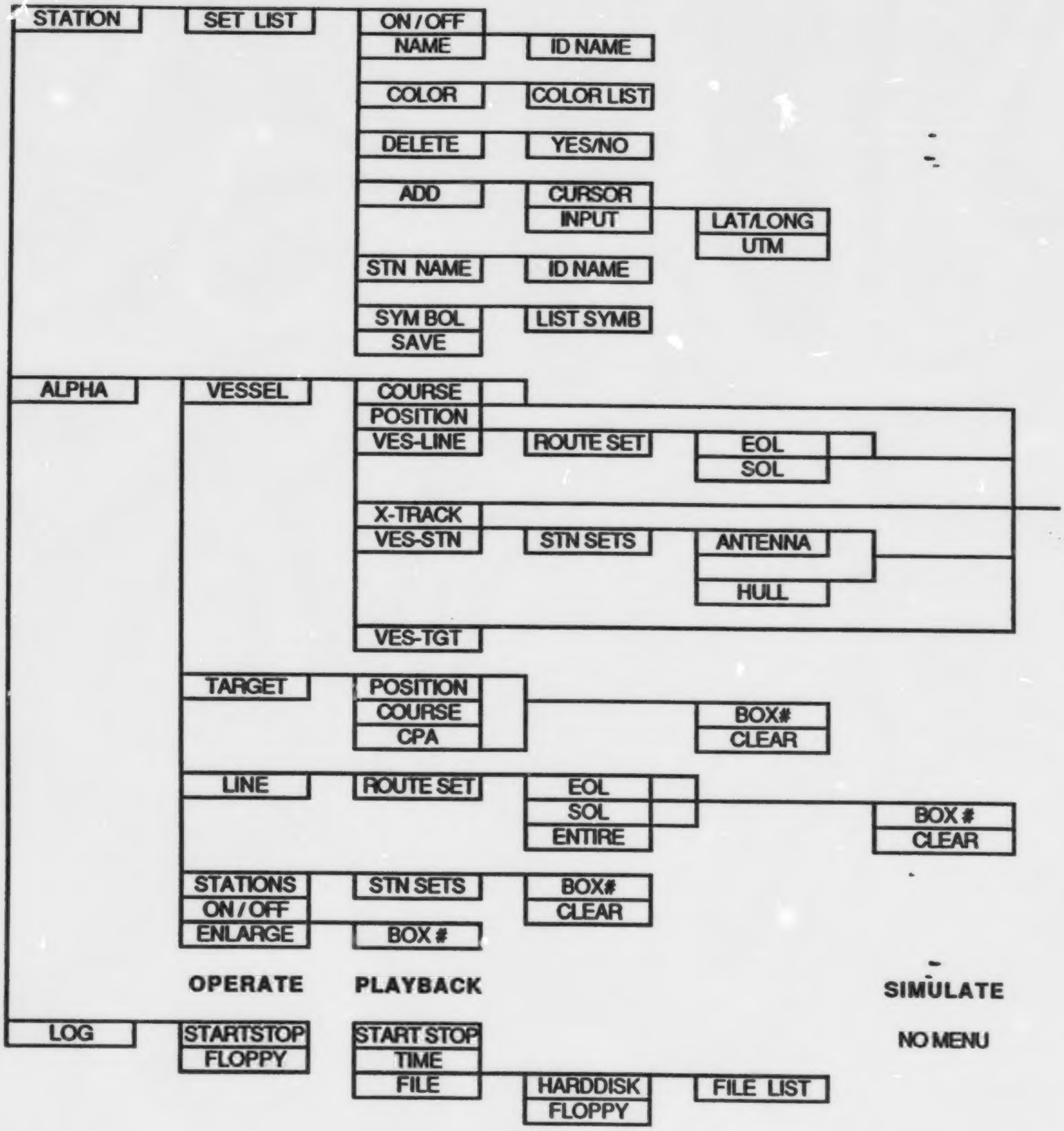

19" RGB monitor screen 360mm x 270mm
1280 x 1024 resolution
Alarm box 360mm x 10 mm
CHART WINDOW
WITH RADAR IMAGE
180mm x 180 mm
CHART WINDOW
180mm x 180 mm
ALPHANUMERIC
DATA
WINDOW
360mm x 65mm
Directed syntax menu box 360mm x 15 mm
ARPA screen 340mm x 340mm

SINADS
DUAL CHART
WITH LOWER
ALPHA
PRESENTATION

Figure 17


HARDKEYS:
SOFTKEYS:
ALARM ACK
RETURN
SCREEN
FILE LIST
SYSTEM
THIS KEY IS NOT ACTIVE
SPECIAL
THIS KEY IS NOT ACTIVE
ZOOM
1/4
1/2
1
1-1/2
3
6
12
ALARM
STATUS
SILENCE
DISABLE
ALARM LIST
MODE
OPERATE
PLAYBACK
SIMULATE
AREA LIST
NAVIGATE
SET LIST
PLAN
SET LIST
ON / OFF
NAME
ID NAME
COLOR
LIST COLOR
REVERSE
DELETE
SET
LINE
YES / NO
ADD
CURSOR
START
END
NODE
SNAP
INPUT
LAT/LONG
UTM
START
NODE
END
SAVE
CHART
FILE LIST
CURSOR
POSITION
VES-CUR
TGT-CUR
LINE-CUR
ROUTE SET
EOL
SOL
STN-CUR
STN SET


RADAR
ON/OFF
MATCH
ROTATE
<<<<
....
>>>>
TRANS-X
<<<<
....
>>>>
TRANS-Y
^^^^
....
vvvv
CONTROLS
GAIN
1 thru 8
STC
1 thru 8
AZM - CLUT
RNG - CLUT
EDGE
BUFFER
SEARCH
OFF
MINIMUM
MAXIMUM
RINGS
TARGET
ACQUIRE
DROP
CPA
100
250
500
1000
2500
5000
10000
20000
GRAPHIC
VESSEL
TRACK
COMPASS
ELLIPSE
VECTORS
EBL
VRM
UNITS
CO-ORDS
UTM
LAT/LONG
RECTANG
POLAR
DISTANCE
METERS
FEET
CABLES
N.MILES
SPEED
KNOTS
M / S
KPH


STATION
SET LIST
ON / OFF
NAME
ID NAME
COLOR
COLOR LIST
DELETE
YES/NO
ADD
CURSOR
INPUT
LAT/LONG
UTM
STN NAME
ID NAME
SYM BOL
SAVE
LIST SYMB
ALPHA
VESSEL
COURSE
POSITION
VES-LINE
ROUTE SET
EOL
SOL
X-TRACK
VES-STN
STN SETS
ANTENNA
HULL
VES-TGT
TARGET
POSITION
COURSE
CPA
BOX#
CLEAR
LINE
ROUTE SET
EOL
SOL
ENTIRE
BOX #
CLEAR
STATIONS
ON / OFF
ENLARGE
STN SETS
BOX#
CLEAR
BOX #
OPERATE
PLAYBACK
SIMULATE
LOG
STARTSTOP
FLOPPY
START STOP
TIME
FILE
HARDDISK
FLOPPY
FILE LIST
NO MENU

Shipboard Integrated Navigation And Display System

SINADS

OPERATOR'S MANUAL

V.1.0

Offshore Systems Ltd • 1974 Spicer Rd • North Vancouver BC • Canada • V7H 1A2

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SINADS COMMANDS

Introduction

The SINADS keyboard and commands are designed for efficiency. To achieve this efficiency, Offshore Systems has divided the commands into two groups: hard keys and soft keys. Hard key commands are fixed, while the soft keys commands are variable. These variable commands are hierarchical, and they appear as a menu tree.

NOTE: **HARD KEYS: IN BOLD AND CAPITALIZED.**
SOFT KEYS: IN PLAIN TEXT AND CAPITALIZED

Hard Keys(See Figure1)

SINADS has 18 hard keys: 16 keys in a keypad and two others--**ALARM ACK** and **RETURN**-- on the far right of the keyboard. Each of the 16 keypad hard keys controls a specific category of commands, eg, chart, cursor, or units. And each category has its menu of variable commands. This menu of variable commands is known as a software menu. Thus each hard key controls its own software menu.

The first step in executing an operation is to select the category of command, eg, zoom, navigate, or radar. Consequently, the first key to be pressed is a hard key. Pressing this hard key produces its software menu. This software menu appears in the eight soft-key windows on the bottom of the

Depending on the complexity of the operation, the software menu can vary from one level (eight selections) to five levels (40 selections) in the present version of SINADS. The eight keys across the top of the keyboard function as the soft keys. The soft-key boxes corresponding to these eight keys appear along the lower edge of the monitor screen (See Fig1).

Note: The label displayed in the soft-key box changes with the hard key and the level of the soft key.

Command Path

The 16 hard keys and their soft keys are 16 independent, command paths. Each command path descends to lower menu levels. Consequently, two questions arise: (a) how to return to a previous (ie, higher) menu level and (b) how to change to another command path.

Return to Previous Menu Level

To return to a previous menu level (ie, higher menu level), the operator presses the **RETURN** key. (See Figure 1). The **RETURN** key is a hard key, and is used for returning up all 16 command paths.

Change Command Paths

A quick way to change command paths is to press the appropriate hard key. For example, an operator is working in the soft key menu of **CHART**, (eg, COLOUR). If the operator presses **RADAR**, the system changes the top level of the **RADAR** menu.

The following pages illustrate the workings of the hard keys and their soft-key menus.

THE RETURN AND ALARM ACKNOWLEDGE KEYS

Introduction

Unlike the 16 hard keys in the hard-keys keypad, the **ALARM ACK** and the **RETURN** are found on the far right of the keyboard. These keys are located in a separate key-pad because of their particular functions. The **ALARM ACK** is located for a prompt response to an alarm. Similarly, since the **RETURN** key is used for returning up all 16 command paths, it is located to the right on its own for fast access.

To return to a previous menu level (ie, a higher menu level), the operator presses the **RETURN** key.

A. Return to Previous Menu Level

To return to a previous menu:

- Press **RETURN.**

B. ALARM ACKNOWLEDGE

This hard key acknowledges the alarm, and temporarily silences the audible signal.

To acknowledge an alarm signal:

- Press **ALARM ACK.**

ALARM

Introduction

The hard key **ALARM** produces a software menu that controls the alarm status and the silencing of the alarms. The soft-key menu tree has three soft keys at the first level: STATUS, SILENCE, and DISABLE.

Determine the Status of an Alarm

- Press **ALARM.**

  ALARM displays a menu consisting of STATUS and SILENCE.

- Press STATUS.

  STATUS displays a list of the alarm categories in the soft-key menu boxes across the bottom of the screen.

- Press a highlighted (ie, activated) alarm.

  The screen displays the first error in that category.

  Pressing the highlighted category again displays the next error in that category.

  This procedure can be repeated until all the errors in that activated category are displayed.

  The end of the list of errors is identified by a message stating, "no more alarms."

Silence Permanently the Audible Alarm Signal

- Press **ALARM.**
- Press SILENCE.
- Select alarm category.

Turns off the audible signal without turning off the alarms. Thus when activated, the alarms continue to flash on the screen.

Note The keys toggle between highlighted (green) and normal (white).

Alarm Colours

The alarms across the top of the screen are displayed in the following colours:

a. blue: alarm inactive;

b. red: alarm active but not acknowledged; and

c. green: alarm active but acknowledged.

Note Restarting the system automatically turns on the audible signal.

Disable the Alarm

- Press **ALARM.**
- Press DISABLE.
- Select alarm category.

Disables the alarm category. The alarm category remains disabled until reselected. The DISABLE key toggles between enable and disable.

ZOOMING

Introduction

The hard key **ZOOM** produces a software menu that controls zooming in and out on the charts. The soft-key menu tree comprises a series of zoom ranges from 1/4 nautical mile to 12 nautical miles. The size of a chart window across its bottom is always twice the selected zoom range.

Zoom In on the Chart

- Press **ZOOM.**

- Select one of the following:

1/4 Indicates that the zoom range is 1/4 nautical mile. The window size across the bottom is 1/2 nautical mile.

1/2 Indicates that the zoom range is 1/2 nautical mile. The window size across the bottom is one (1) nautical mile.

1 Indicates that the zoom range is one (1) nautical mile. The window size across the bottom is two (2) nautical miles.

11/2 Indicates that the zoom range is 1.5 nautical miles. The window size across the bottom is three (3) nautical miles

3 Indicates that the zoom range is three (3) nautical miles. The window size across the bottom is six (6) nautical miles.

6 Indicates that the zoom range is six (6) nautical miles. The window size across the bottom is 12 nautical miles

12 Indicates that the zoom range is 12 nautical miles. The window size across the bottom is 24 nautical miles

Note When one of the ranges is pressed, the keyboard remains locked until the zoom is completed.

MODE

Introduction

The hard key **MODE** produces a software menu that controls the modes available in SINADS. SINADS offers three modes: operate, playback, and simulate.

- Press **MODE.**

EITHER:

- Press OPERATE.

OR:

- Press PLAYBACK.

OR:

- Press SIMULATE.
- Select the operation area, eg, Vancouver, Montreal, etc. from the list of areas.

NAVIGATE

Introduction

The hard key **NAVIGATE** produces a software menu that controls which route set is used for cross tracking. **NAVIGATE** also has a soft key labelled NO-PLAN. Selecting this soft key indicates to the system that no route set is selected. Consequently, the system eliminates cross-track information.

Route Lists

Routes are stored in the system's memory. The files are labelled for easy access. One method of labelling is to name them by geographical area, eg., Vancouver, Nanaimo, Port of Basque, etc. Thus each file contains a list of routes for its area.

Note To create or edit a route, refer to the hard-key plan.

When a route is selected, the system also displays cross-track information.

Note A maximum of 15 sets of routes can be stored in memory.

Select a Route

- Press **NAVIGATE.**

The IDC screen displays a list of route sets stored in the system.

- Select a route set from the list.

Select NO-PLAN

To select NO-PLAN:

- Press **NAVIGATE.**

- Press NO-PLAN.

PLAN

Introduction

The hard key **PLAN** produces a software menu that controls the creating and editing of up to 15 routes.

A route is a set of independent lines. Each line is defined by its start and end point.

Each of the 15 sets can be assigned a name (ID).

A set consists of any number of lines, including zero, (ie, no lines). All lines in a set have the same colour.

Note Lines within a set need not be interconnected.

PLAN has a software menu tree with three levels of commands:

First Level:

The first level offers the list of line (route) sets.

Second Level:

The second level has the following keys:

(1) ON/OFF.

(2) NAME.

Allows each set of stations to be given a name.

Third Level:

(a) an alphabet menu.

Second Level:

(3) COLOR.

Third Level:

(b) a list of colours, and

Second Level:

(4) DELETE.

Third Level:

(c) Yes/No.

Second Level:

(5) ADD.

Third Level:

(d) a list of commands:

(i) START,

(ii) END,

(iii) ACCEPT, and

(iv) SNAP-ON.

And,

Second Level:

(6) SAVE.

Editing Route Sets

SINADS can do the following:

a. turn the display of a set of route lines on or off the screen;

b. change the name (ID) of a set;

c. change the colour of a set of lines;

d. delete the line closest to the cursor in a set;

e. add lines; and

f. save all changes to a file.

Turn a Set On/Off

- Press **PLAN.**
- Select the wanted set.

- Turn the set on (or off).

Change the Name of a Set

- Press **PLAN.**

- Select the wanted set.

- Enter name by using the alphabet menu.

The alphabet menu comprises four boxes with each containing a set of letters:

a. A - H;

b. I - P;

c. Q - X; and

d. YZ?/ ...

To select a letter:

- Use the cursor to highlight a letter.

- Press ENTER on the numeric keyboard.

To erase a letter:

- Press the backspace key.

Note Use the numerical keyboard to select a number.

The name has a maximum of eight characters.

Change the Colour of Lines in Set

- Press **PLAN.**
- Select the wanted set.
- Press COLOUR.
- Select the wanted colour.

Delete the Line Closest to the Cursor

- Press **PLAN.**
- Select the wanted set.
- Press DELETE.

EITHER:

- Press YES [to delete].

OR:

- Press NO.

Add a Line

- Press **PLAN.**

- Select the wanted set.

- Press ADD.

ADD activates another menu level that includes START (of a line), END (of a line), ACCEPT and SNAP-ON.

- Press START. This command displays a marker at the cursor's position.

- Press END. This common displays a marker at the cursor's new position.

- Press ACCEPT. This command creates a line between the two markers.

SNAP-ON **To Join Two Lines**

The command SNAP-ON gives precision when joining two lines. The start of one line has the same value as the end of the other line, thus ensuring that the two lines are "snapped" on without leaving a gap between the ends.

SNAP-ON functions as a toggle switch between SNAP ON and SNAP OFF. When snap is on, the key displays the message SNAP OFF, and when the snap is off, the key displays the message, SNAP-ON.

To use the snap function:

- Press **PLAN.**

- Select the wanted set.

- Press ADD.

- Press SNAP-ON.

- Press START.

Snap can only be used on the set of lines on which the operator is currently working. If a set has no lines, the following message appears: "No lines in set, cursor position used."

Save a Set of Lines

Pressing the SAVE command saves the entire file of lines, ie, all sets, and not just the current set of lines.

- Press **PLAN.**

- Select the wanted set.

- Press SAVE.

CHART

Introduction

Pressing the hard key **CHART** produces a software menu that controls the selection of a chart for display. When **CHART** is pressed a list of all the files appears.

Note When CHART is pressed, the keys remain locked until the chart appears on the screen.

Select a Chart File

- Press **CHART**
- Select a chart file.

CURSOR

Introduction

The cursor serves as a marker used to focus on any object or co-ordinate on the chart.

The hard key **CURSOR** produces a software menu that controls the information in the cursor information box. **CURSOR** activates the soft-key menu tree containing the following soft-keys at the first level:

a. POSITION,

b. YES-CUR,

c. TGT-CUR,

d. LINE-CUR, and

e. STN-CUR.

POSITION

Displays the position of the cursor in the selected co-ordinates system.

YES-CUR

Displays the range and bearing from the vessel to the cursor.

TGT-CUR

Displays the range and bearing from the target to the cursor.

LINE-CUR

Selects the same set list as in PLAN and NAVIGATE.

When a set is selected, the system selects from the set the line closest to the cursor.

Either the start of the line (SOL), or its end (EOL) can be selected for the point from which to measure the distance to the cursor.

Wherever the cursor is moved on the screen, the cursor information box displays the distance from the cursor to the selected point on the line.

STN-CUR

Selects the same station list as in STATION and ALPHA.

The operator selects a set, and whichever station in that set is closest to the cursor is selected.

Wherever the cursor is moved on the screen, the cursor information box displays the distance from the cursor to the selected station.

Display Cursor Position

- Press **CURSOR.**
- Press POSITION.

Display Vessel to Cursor

- Press **CURSOR.**
- Press VES-CUR.

Display Target To Cursor

- Press **CURSOR.**

- Press TGT-CUR.

Display Line to Cursor

- Press **CURSOR.**

- Press LINE-CUR.

- Select the same set list as in PLAN and NAVIGATE.

When a set is selected, the system selects from the set the line closest to the cursor.

To select end of line:

- Press EOL.

To select start of line:

- Press SOL.

Display STATION to Cursor

- Press **CURSOR.**

- Press STN-CUR.

- Select the same station list as in STATION and ALPHA.

  When a set is selected, the system selects from the set the station closest to the cursor.

RADAR

Introduction

The hard key **RADAR** produces a software menu that controls the radar display on the screen. The software menu has the following soft keys at the first, second, and third levels:

First Level:

a. ON/OFF.

Toggles on and off the radar display on the screen.

First Level:

b. MATCH.

Allows the operator to rotate or translate the radar so that it matches the chart on the screen.

Second Level:

(1) ROTATE.

Gives the angle of rotation that is required to ensure that the radar image matches the chart on the screen.

Second Level:

(2) TRANS- X.

Gives the offset value in X co-ordinates required to ensure that the radar image matches the chart on the screen.

(3) TRANS-Y.

Gives the offset value in Y co-ordinates required to ensure that the radar image matches the chart on the screen.

First Level:

c. CONTROLS

CONTROLS gives the operator similar control over the radar through the use of the soft keys as through the use of the dials on the radar console. The command activates the following radar controls:

Second Level:

(4) Gain.

Allows the gain to be adjusted.

Third Level:

(a) 1 THRU 8

Indicates the gain range.

Second Level:

(5) STC. (Standard Time Constant.)

Allows for the amplification or attenuation of signals. Toggles between ON and OFF.

Third Level:

(b) LENGTH

Modifies the length of the STC curve.

(c) HEIGHT

Modifies the height of the STC curve.

Both these commands activate a fourth level command: "1-8". This command gives the range of modification-available to the operator.

Second Level:

(6) AZM-CLUT.

Toggles between highlighting AZIMUTH ON and AZIMUTH OFF. AZIMUTH ON turns on the azimuth clutter, which averages the value from four adjacent radials. AZIMUTH OFF takes the value from one radial only.

(7) RNG-CLUT.

Toggles between highlighting RANGE ON and RANGE OFF. RANGE ON takes a running average along the radial of three adjacent values.

(8) Edge.

Highlights the edge of the target in the radar image. Highlighting indicates if the selection is on or off.

(9) BUFF-AVG.

Toggles between highlighting BUFFER ON and BUFFER OFF. BUFFER ON allows averaging between the current value and the old (previous) value of the radar reading. The average reading is then put in memory. With BUFFER OFF, no averaging occurs. And

(10) SEARCH.

Activates another menu with OFF, MIN, and MAX. MAX picks the maximum value between the new and old value and puts it in the buffer. MIN selects the smallest value compared to the old value. OFF turns off this activity.

Third Level:

(d) OFF

Turns off the SEARCH activity.

(e) MAXIMUM

Picks the maximum value and puts it in the buffer.

(f) MINIMUM

Picks the minimum value and puts it in the buffer.

First Level:

d. RINGS.

Turns range rings on or off.

First Level:

e. TARGET.

Second Level:

(g) ACQUIRE

Allows cursor to be fixed on radar image for tracking.

(h) DROP

Releases cursor from tracked radar image.

(i) CPA

Sets an alarm to be activated when the target enters a selected distance.

Turn Radar Display On [or Off]

To turn radar on [or off]:

- Press **RADAR.**

- Press ON [or OFF].

Match Radar To Chart : Rotate Radar Image

The following procedure allows matching of topographic features by rotating the radar image:

- Press **RADAR.**

- Press MATCH.

- Press ROTATE.

The eight soft-key boxes display sets of greater-than (>>>>) and less-than (<<<<) symbols. The number of symbols in a soft-key box indicates the proportional increment (or decrement). The range is from four symbols (<<<<) to one symbol (<) in either direction.

To increase the angle of rotation when matching the radar image with the chart:

- Press an increment box (ie, (>), (>>), (>>>), or (>>>>).

To decrease the angle of rotation when matching the radar image with the chart:

- Press a decrement box (ie, (<) , (<<), (<<<), or (<<<<).

Match Radar To Chart: Translate Radar Image

The following procedure allows matching of topographic features by translating the radar image into X and Y co-ordinates:

To translate radar image into X co-ordinates:

- Press **RADAR.**

- Press MATCH.

- Press TRANS-X

The eight soft-key boxes display sets of greater-than (>>>>) and less-than (<<<<) symbols. The number of symbols in a soft-key box indicates the proportional increment (or decrement). The range is from four symbols (<<<<) to one symbol (<) in either direction.

To increase the offset in X co-ordinates required to match the radar image with the chart:

- Press an increment box (ie, (>), (>>), (>>>), or (>>>>).

To decrease the offset in X co-ordinates required to match the radar image with the chart:

- Press a decrement box (ie, (<) , (<<), (<<<), or (<<<<).

To translate radar image into Y co-ordinates:

- Press **RADAR.**

- Press MATCH.

- Press TRANS-Y

The eight soft-key boxes display sets of symbols that look like a V or its inversion. (The number of symbols in a soft-key box indicates the proportional increment (or decrement). The range is from four symbols (VVVV) to one symbol (V) in either direction.

To increase the offset in Y co-ordinates required to match the radar image with the chart:

- Press an increment box (ie, (V), (VV), (VVV), or (VVVV).

To decrease the offset in Y co-ordinates required to match the radar image with the chart:

- Press a decrement box (ie, (∧) , (∧ ∧), (∧∧∧), or (∧∧∧∧).

Change the Gain

The following procedure allows the gain to be changed:

- Press **RADAR.**
- Press CONTROLS.
- Press GAIN.
- Change the gain level between 1 thru 8.

Change the STC (Standard Time Constant.)

The following procedure allows for the amplification or attenuation of signals:

- Press **RADAR.**
- Press CONTROLS.
- Press STC.
- Select LENGTH. ***OR:***
- Select HEIGHT.
- Change the length or the height of the STC curve between the values of 1 thru 8.

Turn on the Azimuth Clutter

The following procedure turns on the azimuth clutter:

- Press **RADAR.**

- Press CONTROLS.

- Press AZM-CLUT.

The azimuth command toggles between highlighting AZIMUTH ON and AZIMUTH OFF.

Set Range Clutter

The following procedure sets the range clutter:

- Press **RADAR.**

- Press CONTROLS.

- Press RNG-CLUT.

The range command toggles between highlighting RANGE ON and RANGE OFF.

Enhance Edge of Target

The following procedure highlights the edge of the target in the radar image:

- Press **RADAR.**

- Press CONTROLS.

- Press EDGE.

The EDGE command toggles between highlighting EDGE ON and EDGE OFF.

Set BUFFER

The following procedure allows averaging between the current value and the old (previous) value of the radar reading.

- Press **RADAR.**
- Press CONTROLS.
- Press BUFFER.

The BUFFER command toggles between highlighting BUFFER ON and BUFFER OFF.

Hunt for Target

The following procedure activates another menu with OFF, MIN, and MAX:

- Press **RADAR.**
- Press CONTROLS.
- Press SEARCH.

EITHER:

To select the maximum value between the new and old value and put it in the buffer:

- Press MAXIMUM.

OR:

To select the smallest value compared to the old value and put it in the buffer:

- Press MINIMUM.

To turn off the search:

- Press OFF.

Turn Range Rings On (OFF)

- Press **RADAR.**
- Press RINGS

The RINGS command toggles between highlighting ON and OFF.

Select/Drop and Set Alarm Targets

- Press **RADAR.**
- Press TARGETS *EITHER:*

To select a target:

- Press ACQUIRE. *OR:*

To drop a target:

- Press DROP. *OR:*

To select a target range by selecting the closest point of approach (CPA):

- Press CPA.
- Select a range. Ranges vary from 100 m to 20,000 m.

UNITS

Introduction

The hard key **UNITS** produces a software menu that controls the choice of units used in the display of co-ordinates, distance, and speed. The first level of the software menu has the following soft keys:

a. CO-ORDS,

b. DISTANCE, and

c. SPEED.

The second level of the software menu has the following soft keys:

For co-ordinates:

a. UTM,

b. LAT/LONG,

c. RECTANG, and

d. POLAR.

For distance:

a. METERS,

b. FEET, and

c. CABLES.

For speed:

a. KNOTS,

b. M/S, and

c. KPH.

Co-ordinates

Co-ordinates can be displayed in the information boxes in the following units:

a. UTM,

b. lat/long,

c. local grid, and

d. local polar.

Local Grid and Local Polar

Unlike a universal grid such as UTM and Lat/Long, a local grid has a user selected origin. A local grid can be displayed in rectangular or polar co-ordinates (R, ø° ; R=radius and ø=angle measured from the vertical).

A local polar is a local grid described in polar co-ordinates.

Distance

Distance measurements can be displayed in the information boxes in the following units:

a. meters,

b. feet, and

c. cables.

Speed

Speed measurements can be displayed in the information boxes in the following units:

a. knots,

b. meters/sec, and

c. kilomtrs/hour.

Change the Co-ordinate Units

The following procedure displays co-ordinates in the information boxes in the selected units:

- Press **UNITS.**

- Press CO-ORDS.

EITHER:

- Press UTM.

OR:

- Press LAT/LONG.

OR:

- Press RECTANG.

OR:

- Press POLAR.

Select Meters/Feet/Cables

The following procedure displays distance measurements in meters or feet.

- Press **UNITS.**
- Press DISTANCE.

EITHER:

- Press METERS.

Or :

- Press FEET.

Or :

- Press CABLES.

Select Knots/Or Meters/Sec/Or Kilometers/Hour

The following procedure displays speed measurements in knots or meters/sec or kilometers/hour:

- Press **UNITS.**
- Press SPEED.

EITHER:

- Press KNOTS.

OR:

- Press M/S.

OR:

- Press KPH.

STATIONS

Introduction

A station is a point with an X and a Y coordinate.

The hard key **STATIONS** produces a software menu that controls the display and creation of stations on the screen. The software menu tree has three levels of commands:

First Level:

The first level offers the list of station sets.

Second Level:

The second level has the following keys:

(1) ON/OFF.

(2) NAME.
Allows each set of stations to be given a name.

Third Level:

(a) an alphabet menu.

Second Level:

(3) COLOR.

Third Level:

(b) a list of colours.

Second Level:

(4) DELETE.

Third Level:

(c) Yes/No.

Second Level:

(5) ADD.

(6) STN-NAME,

Allows each station to be given a name.

Third Level:

(d) an alphabet menu.

Second Level:

(7) SYMBOL,

Allows the operator to change the station symbol.

Third Level:

(e) a list of symbols.

Second Level:

(8) SAVE.

Stations are organized into sets. These station sets are then labelled for better organization. Stations can:

a. be added;

b. be deleted;

c. have their colours changed;

d. have their shapes changed; and

e. be named.

Turn Station Set On/Off

The selected station set can be displayed on the screen (ON) or turned OFF. When turned off, the stations are no longer visible, but they are still present in memory.

- Press **STATION.**
- Select station set.
- Press ON. ([or OFF].

Name a Set of Stations

- Press **STATION.**
- Select station set.
- Press NAME.
- Enter name.

The name has a maximum of eight characters.

Change the Colour of the Station Set

- Press **STATION.**
- Select station set.
- Press COLOR.
- Select colour.

Delete Station Set

- Press **STATION.**
- Select station set.
- Press DELETE.
- Press YES [to delete]. ***EITHER:***
- Press NO. ***OR:***

Add a Station

- Press **STATION.**
- Select station set.
- Press ADD.

Name a Station

- Press **STATION.**
- Select station set.
- Press STN-NAME.
- Enter name.

The name has a maximum of eight characters.

Change Station Symbol

- Press **STATION.**
- Select station set.
- Press SYMBOL.
- Select symbol from list.

Save Station Set

When the SAVE command is pressed, the entire file of sets, ie, all sets, and not just the current set of stations is saved.

- Press **STATION.**
- Select station set.
- Press SAVE.

ALPHA

Introduction

The hard key **ALPHA** produces a software menu that controls what information is displayed in which information display box on the screen.

The information displayed concerns the following:

a. vessel;

b. target;

c. line; and

d. stations.

The software menu also controls the following:

a. turning the information on/off; and

b. enlarging the information display.

The software menu has the following soft keys at the first level:

First Level:

a. VESSEL

Allows information concerning the vessel's course, position, and range and bearing to other objects to appear in the information boxes.

Second Level:

(1). COURSE.

Allows information about the course to be displayed in any of the information boxes. Information displayed concerns the vessel's speed, course made good, gyro, and speed over ground.

Third Level:

(a) list of boxes.

(b) CLEAR.

Clears the information in the information boxes.

Second Level:

(2). POSITION.

Displays the position of the the vessel in the selected information box.

Third Level:

(a) list of boxes.

(b) CLEAR.

Second Level:

(3). VES-LINE.

Allows the display of information concerning a route (line).

Third Level:

(c) List of Plans.

Fourth Level:

(i) EOL

Fifth Level:

(a1). list of boxes.

(b2). CLEAR.

Fourth Level:
(ii) SOL

Fifth Level:

(a1). list of boxes.

(b2). CLEAR.

Note that whichever line is closest to the cursor is displayed on the screen.

Either the start of the line (SOL) or its end (EOL) can be selected for the point from which to measure the distance to the vessel.

Second Level:

(4). VES-STN.

Selects whichever station is closest to the cursor. The operator can measure from the antenna (source of the microwave) or from the hull.

Third Level:

(d) ANTENNA.

Gives the measurement from the antenna (source of the microwaves) to the station.

(e) HULL.

Gives the measurement from the vessel's hull to the station.

Fourth Level:

(iii) List of Plans.

Fifth Level:

(a1). list of boxes.

(b2). CLEAR.

Second Level:

(5). X-TRACK.

Selects the line closest to the vessel and offers a choice of information boxes in which to place the cross-track information. Note that the set was already selected under NAVIGATE.

Third Level:

(a) list of boxes.

(b) CLEAR.

Second Level:

(6). VES-TGT.

Displays the distance and bearing between the vessel and the selected target.

Third Level:

(a) list of boxes.

(b) CLEAR.

First Level:

b.TARGET

Selects target.

Second Level:

(1). COURSE.

(2). POSITION.

Third Level:

(a) list of boxes.

(b) CLEAR.

First Level:

c. LINE

Displays the line closest to the cursor, and offers a choice of information boxes in which to place the information about the end of the line (EOL), the start of the line (SOL), or the entire line (ENTIRE).

Second Level:

(7) List of Plans.

Third Level:

(f) EOL

Fourth Level:

(iv) list of boxes

(v) CLEAR

Third Level:

(g) SOL

Fourth Level:

(iv) list of boxes

(v) CLEAR

Third Level:

(h) ENTIRE.

Gives such information as bearing and length of a line.

First Level:

d. STATIONS

Displays the station closest to the cursor, and offers a choice of information boxes in which to place the information about the station to the hull or antenna.

Second Level:

(8) List of Stations.

Third Level:

(a) list of boxes.

(b) CLEAR.

First Level:

e. ON/OFF

Turns off all alpha display in the information boxes and the cursor from the screen.

First Level:

f. ENLARGE

Enlarges the display in one or all of the information boxes.

Second Level:

(9) List of Boxes.

Note that each box has a maximum of five lines of information. Enlarging removes some of these lines. Hence not all the information is displayed in the box(es) when enlarged.

Display Vessel's Course

- Press **ALPHA.**

- Press VESSEL.

- Press COURSE.

To select a box for displaying the vessel's course:
- Press BOX #.

OR:

To clear box:
- Press CLEAR.

Display Vessel's Position

- Press **ALPHA.**

- Press VESSEL.

- Press POSITION.

To select a box for displaying the vessel's position:
- Press BOX #

OR:

To clear box:
- Press CLEAR.

Display Vessel to Line

The range and bearing information can be displayed for end-of-line or start-of-line.

- Press **ALPHA.**

- Press VESSEL.

- Press VES-LINE.

- Select a line (route) set.

- Select a line by moving the cursor close to the line.

- Press EOL. [for end-of-line]

OR:

- Press SOL. [for start-of-line]

To select a box for displaying vessel-to-line data:
- Press BOX #.

OR:

To clear box:
- Press CLEAR.

Display Vessel to Station

The range and bearing data for a station can be measured from the antenna or from the closest part of the vessel.

- Press **ALPHA.**

- Press VESSEL.

- Press VES-STN.

- Select a station set.

- Select a station by moving the cursor close to the station.

- Press ANTENNA.

- Press HULL.

To select a box for displaying vessel-to-station data:
- Press BOX #

To clear box:
- Press CLEAR.

Select Cross Track

- Press **ALPHA.**

- Press VESSEL.

- Press X-TRACK.

To select a box for displaying cross-track data:
- Press BOX #.

To clear box:
- Press CLEAR.

Display Vessel to Target

- Press **ALPHA.**

- Press VES-TGT.

To select a box for displaying vessel to target data:
- Press BOX #.

To clear box:
- Press CLEAR.

Display Target's Position

- Press **ALPHA.**

- Press TARGET.

- Press POSITION.

To select a box for displaying the target's position:

EITHER:

OR:

OR:

OR:

OR:

- Press BOX #.

To clear box:
- Press CLEAR.

OR:

Display Target's Course

- Press **ALPHA.**
- Press TARGET.
- Press COURSE.

To select a box for displaying the target's course:
- Press BOX #

OR:

To clear box:
- Press CLEAR.

Display Line

- Press **ALPHA.**
- Press LINE.
- Select a line (route) set.
- Select a line by moving the cursor close to the line.

EITHER:

- Press EOL. [for end-of-line]

OR:

- Press SOL. [for start-of-line]

OR:

- Press ENTIRE. [for entire line]

To select a box for displaying line data:
- Press BOX #

OR:

To clear box:
- Press CLEAR.

Display Information About a Station

- Press **ALPHA.**
- Press STATIONS.
- Select a station set.
- Select a station by moving cursor close to the station.

To select a box for displaying station data:
- Press BOX #.

OR:

To clear box:
- Press CLEAR.

Clear Information Boxes

- Press **ALPHA.**
- Press OFF. The key is an OFF/ON key.

Enlarge Information in Information Boxes

- Press **ALPHA.**
- Press ENLARGE.
- Select box.

LOG

Introduction

The hard key LOG produces one of three software menus. The software menu displayed depends on the selected mode, because each mode has its own software menu. Note that the operator selects a mode at start up.

In OPERATE, the soft keys are START/STOP and FLOPPY. These keys have the following function:

START/STOP

Starts or stops recording.

FLOPPY

Allows any of the five files on the hard disk to be saved on a floppy disk.

In PLAYBACK, the soft keys are START/STOP, TIME, and FILE. These keys have the following function:

START/STOP

Starts or stops playback.

TIME

Allows the time of the playback to be changed.

FILE

Changes the source of information in playback, ie, changes the file used.

HARD DISK

Allows playback from one of the five files on the hard disk.

FLOPPY

Allows playback from the file on the floppy disk. Note that the floppy disk has only one file.

In SIMULATE, the soft-key command does not produce a menu. The status message prints, "LOG INACTIVE: IN SIMULATION MODE."
INACTIVE.

Start Recording

When recording a new operation:

- Press **LOG.**

- Press START.

Stop Recording

- Press **LOG.**

- Press STOP.

Save Recording on a Floppy

- Press **LOG.**

- Press FLOPPY.

Start/Stop Playback

Note If the mode needs to be changed, refer to the hard key **MODE.**

- Press **LOG.**
- Press START. The key is a START/STOP key.

Time for Playback

Note If the mode needs to be changed, refer to the hard key **MODE.**

- Press **LOG.**
- Press TIME.

Change File in Playback

Note If the mode needs to be changed, refer to the hard key **MODE.**

- Press **LOG.**
- Press FILE.

Either:

- Press HARD DISK.

Or:

- Press FLOPPY.
- Select file from list.

GRAPHICS

Introduction

The hard key **GRAPHICS** allows the operator to select for graphic display a series of outlines. Thus pressing **GRAPHICS** produces the following software menu:

a. Vessel;

b. Track;

c. Compass;

d. Ellipse; and

e. Vectors.

Select Vessel Outline

- Press **GRAPHICS.**

- Press VESSEL.

Select Track Outline

- Press **GRAPHICS.**

- Press TRACK.

Select Compass

- Press **GRAPHICS.**

- Press COMPASS. A circle with divisions indicating degrees appears on the screen.

Select Ellipse

- Press **GRAPHICS.**
- Press ELLIPSE.

Produces an error ellipse for the vessel's position.

Select Vectors

- Press **GRAPHICS.**
- Press VECTORS.

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APPENDIX G - SINADS VESSEL POSITIONING

g1. SINADS Positioning Algorithm

The SINADS positioning algorithm is extensively tested using both simulated and real positioning data. It contains three major components:

a) RANGE task;

b) OBSERVATION task, and

c) POSITION task

The philosophy of the algorithm design is such that any type of measurement obtainable in real-time can be entered as an observation into the position determination process. Currently, only line-of-sight microwave, gyro and speed log are incorporated; however, the design allows for GPS, Loran C, Transit, acoustic and other ranging systems (eg ARGO) to be integrated into the system with minimal additional software development. The output consists of ship's velocity (SOG), water current and direction, heading (CMG), and a position in UTM with corresponding 95% error ellipses. Other information derivable from these results include distance off-line (if following a track), distance and course to pre-selected waypoints, ETA, drift direction and velocity, etc.

g1.1. RANGE Task

Readings of the various data inputs are obtained as fast as they are presented with unprocessed observations being discarded as newer ones become available. This ensures that the positioning algorithm will only use the most recent data. Each data input is polled in a serial fashion. If no new data is available from a specific device, then that observation type will not be used in the next iteration of the positioning procedure. If a device does not respond or produce a valid response for a configurable number of polls, an alarm is set. If most or all the devices fail to respond in a polling iteration, the positioning algorithm will use whatever is available to calculate the most probable position update. The only device that must respond in every iteration is the system clock, and no polling will take place until this information is received.

g1.2. OBSERVATION PROCESSING Task

This part of the algorithm takes the raw data inputs available for the current iteration and reduces them to a form that the positioning procedure can use with no further computations. The processing includes:

a) slope distance reduction;
b) antenna(s) offset corrections;
c) map projection reductions;
d) geodetic corrections (earth curvature, etc.);
e) unit conversions (knots -> m/sec; degrees -> radians);
f) atmospheric and/or acoustic correction facts; and
g) estimation of observation variances.

This module also monitors the integrity of the raw data and activates alarms if poor quality data is received over a configurable number of inputs. As a first approximation, the poor quality data is that which is more than 3 standard deviations from its predicted value.

g1.3. POSITION Task

The main positioning method incorporates a Kalman filter type algorithm with six states. These include the ship's position in x and y, its velocity in x and y, and the current's velocity in x and y. Any number (including 0) of observations may be processed during one iteration. If there is one or no ranges (but possibly gyro and/or speed log data is being processed) then this is equivalent to dead-reckoning for one fix. Simulations have shown this filter to produce excellent results for extended periods of dead-reckoning, especially when changes in heading and velocity are minimal; however when reliable ranges are re-introduced, this filter can be slow to respond, and more so if large maneuvers have taken place during the dead-reckoning period. To overcome this situation a method has been devised to improve considerably the filter's performance. This method consists of computing a traditional, least-squares position and treating it as an "observation" with a large weight (ie zero variance). Several of these observations in a row significantly improve the filter's ability to respond after a period of dead-reckoning and maneuvering.

Alarms are activated when dead-reckoning has taken place either for a configurable number of position updates or when the error ellipse parameters of the computed position exceed a threshold level.

A detailed description of methods used in the design of SINADS positioning filter can be found in [3], [4],[5], and [6].

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APPENDIX H - SINADS RADAR SCAN CONVERTER

This Appendix contains the final version of the SINADS Radar Scan Converter user's manual. The manual presents both the principals of operation of the RSC as well as the technical details of it's design.

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SINADS RADAR SCAN CONVERTER SUBSYSTEM
FINAL VERSION

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1. OVERVIEW OF SINADS CIRCUIT BOARDS
2. BUFFER CIRCUIT BOARD DESCRIPTION
3. CONVERTER CIRCUIT BOARD DESCRIPTION
4. DIGITIZER CIRCUIT BOARD DESCRIPTION
5. SYNCHRO CIRCUIT BOARD DESCRIPTION
6. DIRECTIONS ON USE OF RADAR COMPONENTS

APPENDIX

A EPROM GENERATING PROGRAM

B PAL EQUATIONS

C CRT5037 DATA SHEET

D CIRCUIT BOARD ECO's

E CIRCUIT BOARD SCHEMATICS

INTEGRAD TECHNOLOGIES INC. DORION, QUEBEC . DECEMBER 1988

1.1 OVERVIEW OF SINADS CIRCUIT BOARDS

There are four printed circuit boards in the radar subsystem;

a. BUFFER board
b. CONVERTER board
c. DIGITIZER board
d. SYNCHRO board

These four circuit boards comprise, with a local processor board, a complete radar digitizing, processing and storage subsystem with raster scan diagnostic display. The circuit boards are designed to employ the industry standard double Eurocard form factor and to interface to a local processor board utilising the Motorola MVMX32 bus as well as a subset of the VSB bus. Both these busses are high speed 32 bit address and data interfaces to, among others, the Motorola 68020 and 68030 based families of single board computers. The BUFFER and CONVERTER boards have the MVMX32 interface with DIP-switch selectable addressing. The BUFFER, CONVERTER and DIGITIZER boards communicate with each other over a proprietary synchronous bus using the 96-pin P1 connector and a 3-slot VME backplane. The SYNCHRO board provides a 14-bit digital antenna position word to the CONVERTER board on a 26-pin ribbon cable.

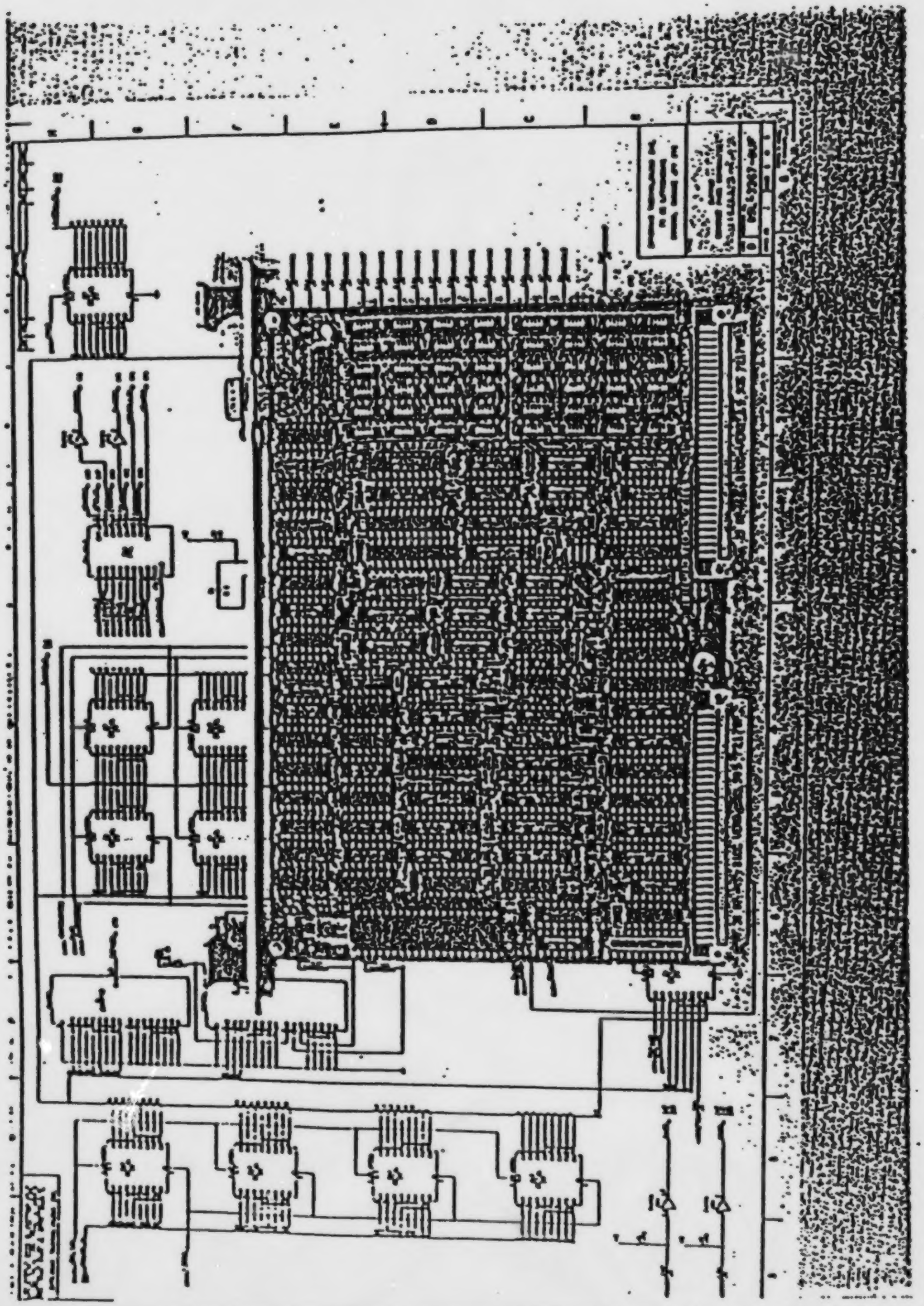
The required inputs to the sub-system are;

a. Radar video (d.c. demodulated radar Rx output)
b. Radar trigger
c. Synchro, Resolver or Direct Sine, Cosine antenna positioning signals

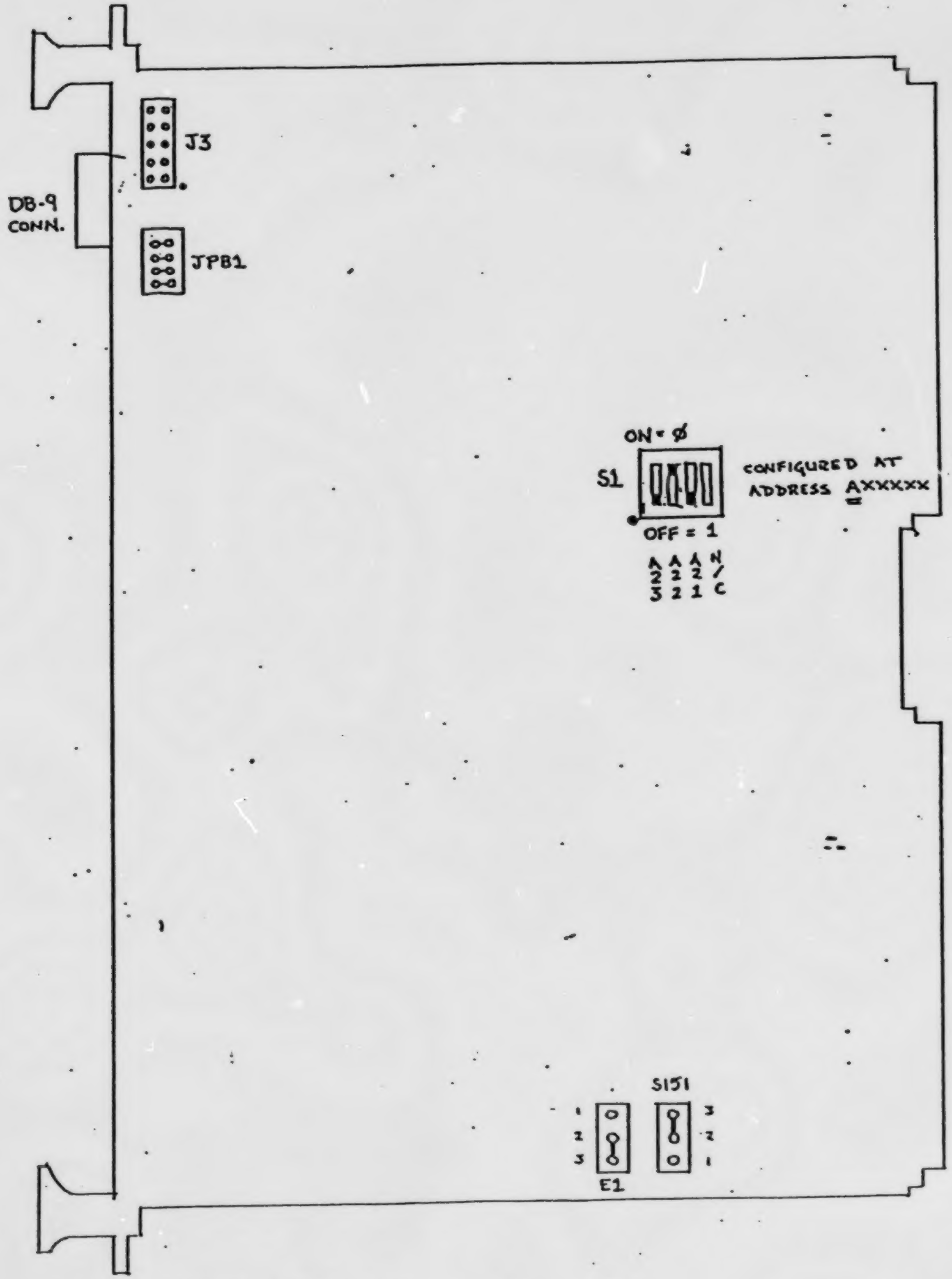
The outputs of the sub-system are;

a. 1024 by 1024 by 8-bit X,Y Cartesian Radar image
b. 1024 by 1024 by 2-bit raster scan Diagnostic video
c. 14-bit Antenna position word

BUFFER BOARD (component side)

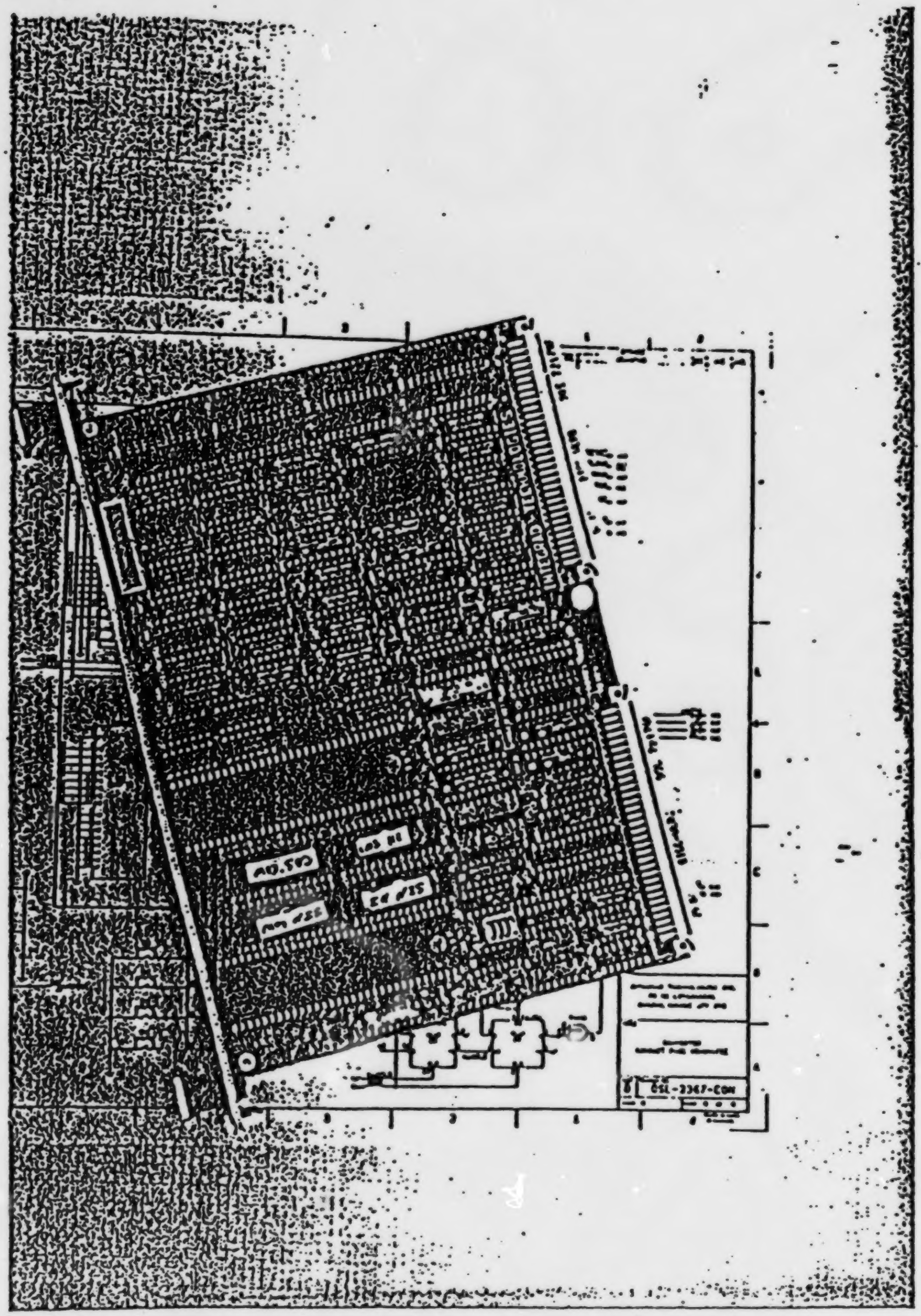


BUFFER BOARD OUTLINE

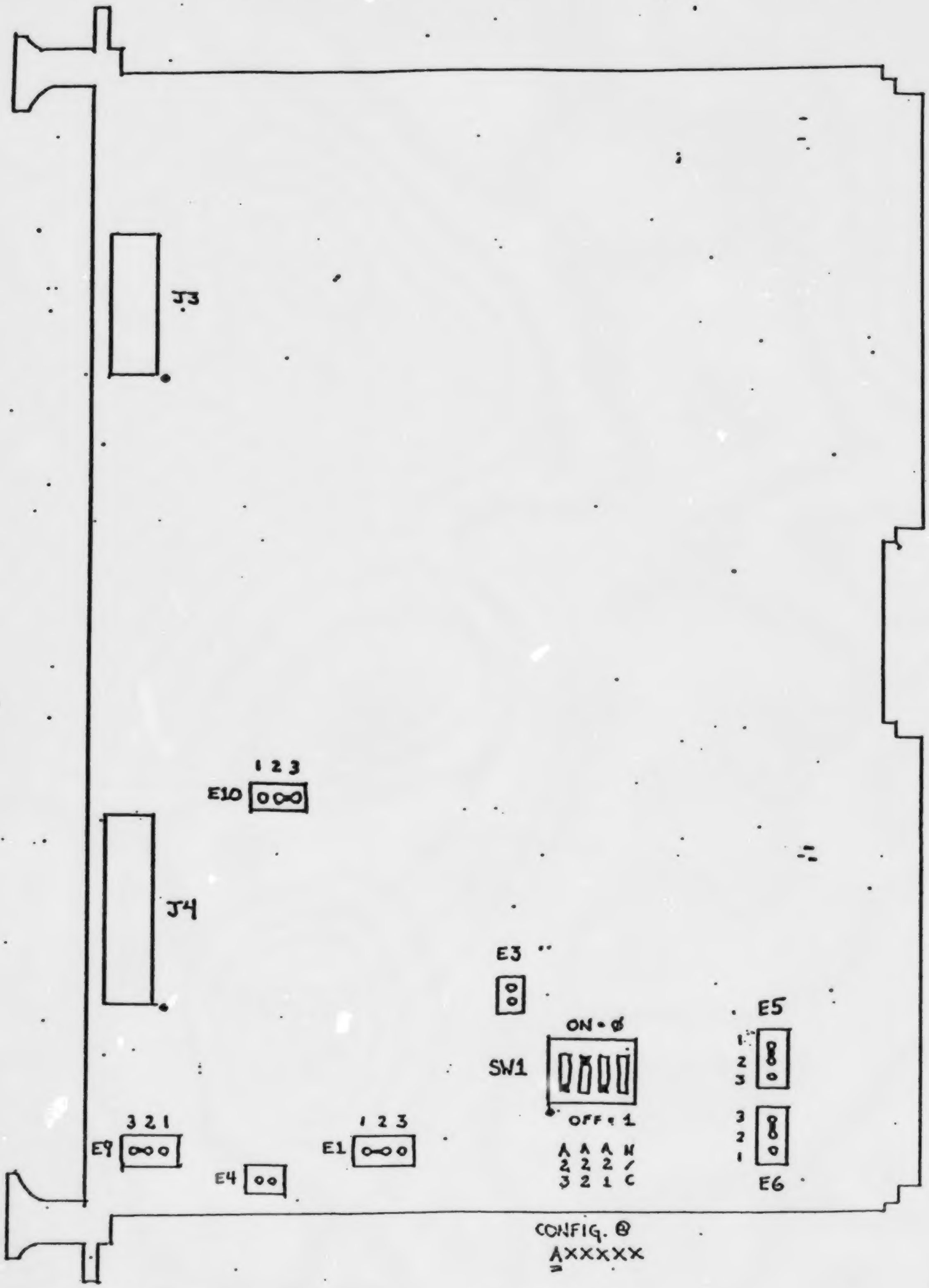

J3
DB-9 CONN.
JPB1
ON = 0
S1
CONFIGURED AT ADDRESS AXXXXX
OFF = 1
A23 A22 A21 N/C
S1S1
3 2 1
1 2 3
E1

OVERVIEW OF SINADS CIRCUIT BOARDS page 1.3

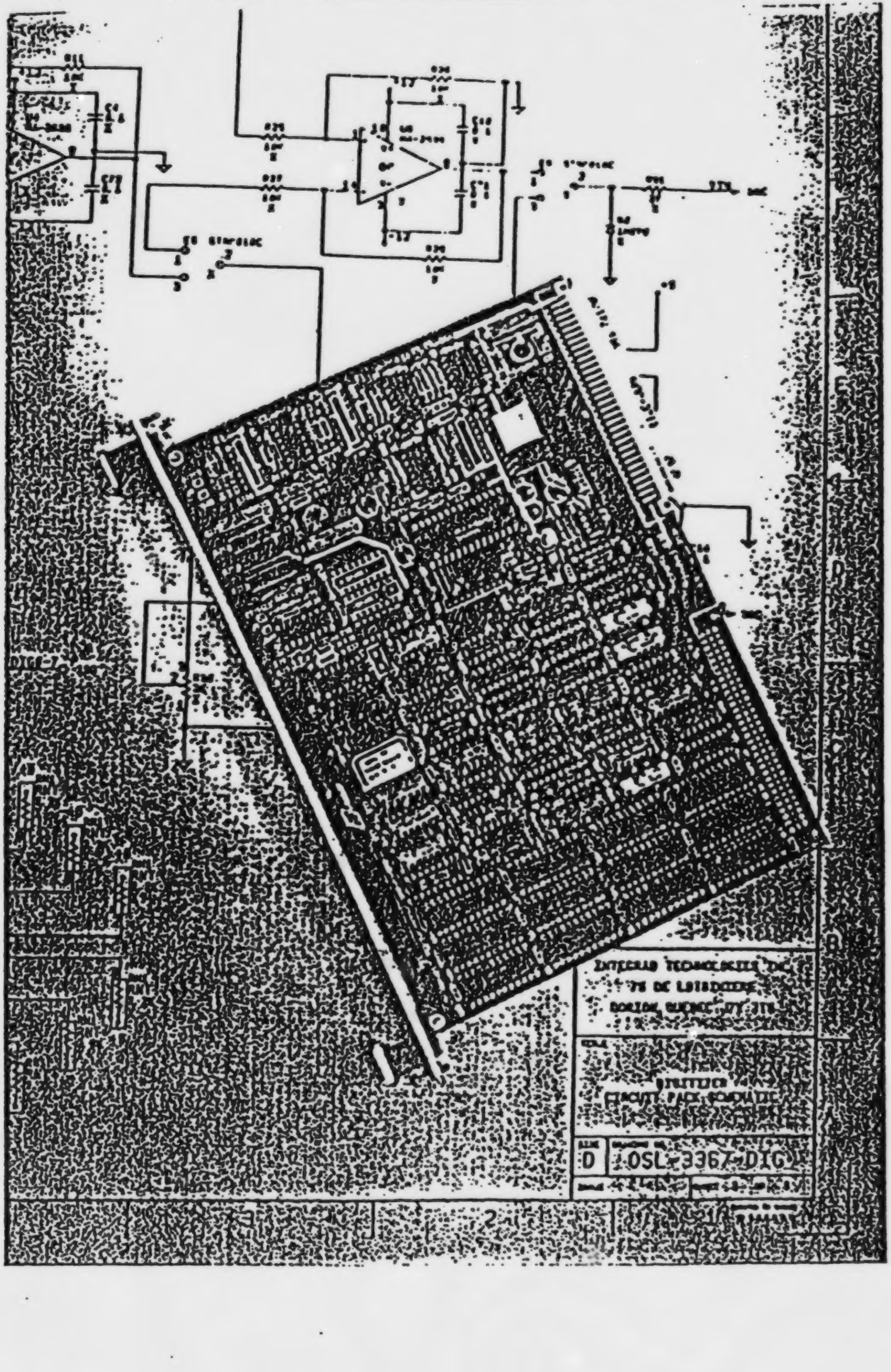
CONVERTER BOARD



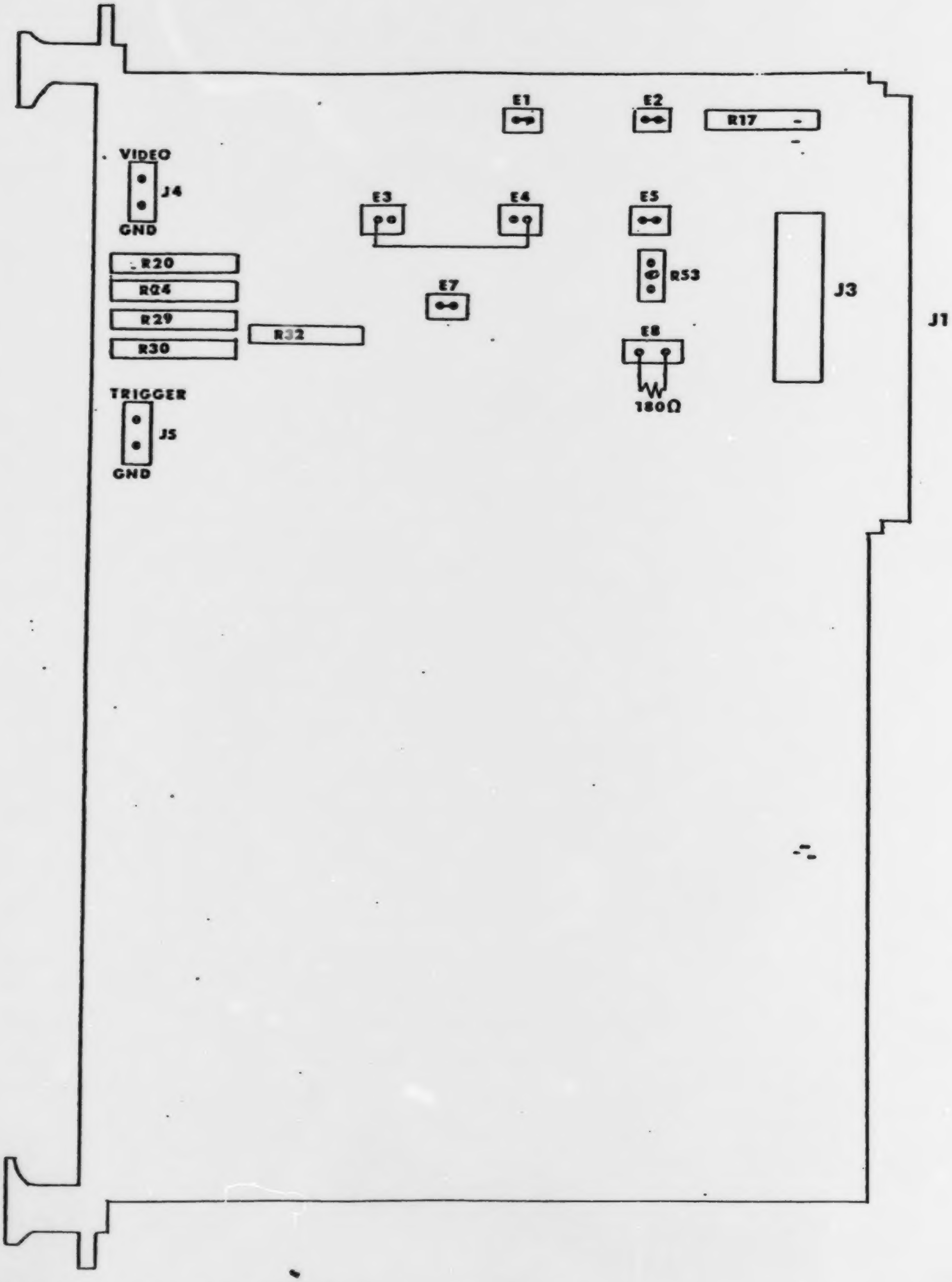
CONVERTER BOARD OUTLINE


J3
1 2 3
E10
J4
E3
ON • 0
SW1
OFF • 1
A A A N
2 2 2 /
3 2 1 C
E5
1
2
3
3
2
1
E6
3 2 1
E9
E4
1 2 3
E1
CONFIG. 0
AXXXXX

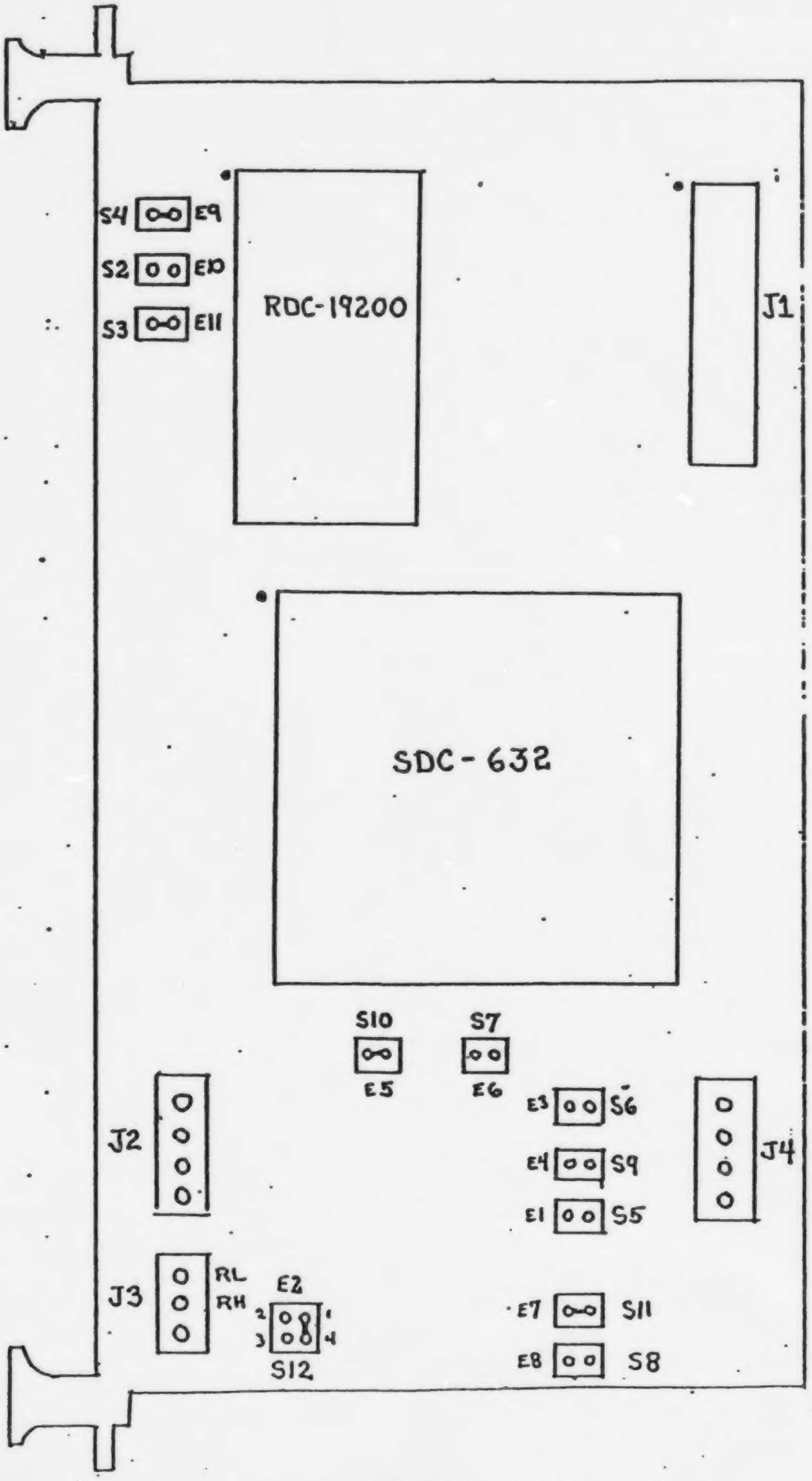
DIGITIZER BOARD


DIGITIZER
CIRCUIT PACK SCHEMATIC
D
OSL-3367-DIG
2

DIGITIZER BOARD OUTLINE (rev 1.0)


E1
E2
R17
VIDEO
J4
GND
E3
E4
E5
R53
J3
J1
E7
R20
R24
R29
R30
R32
E8
180Ω
TRIGGER
J5
GND

SYNCHRO BOARD OUTLINE



S4
E9
S2
E10
S3
E11
RDC-19200
J1
SDC-632
S10
E5
S7
E6
E3
S6
E4
S9
E1
S5
J2
J4
J3
RL
RH
E2
2
1
3
4
S12
E7
S11
E8
S8

2.1. BUFFER BOARD OVERVIEW

The BUFFER board is comprised of two memory arrays designed to interface with its companion CONVERTER and DIGITIZER boards to store and display radar data in a raster scan (X,Y) format. The two data storage arrays are identified as the RAB and RIB memories. The RAB memory is organised as a 1024 by 1024 by-8-bit (256 level) array used to store the 8-bit radar data digitized by the DIGITIZER and processed and scan converted by the CONVERTER boards. The RAB maintains the full 8-bit data word size generated by the DIGITIZER. The RIB memory is organised as a 1024 by 1024 by 2-bit (4 level) array used to store a selected 2-bits (contiguous) out of the 8 bits being stored in the RAB. As will be seen, this allows the local radar processor to read back the RIB radar data at a rate four times that of the RAB. The RIB memory is also connected to an onboard CRT controller to produce a diagnostic video display of the radar data. This display conforms to conventional RGB-type video presentations as a 512 Horizontal by 512 Vertical, 30 Hz interlaced, 2 bit video signal with separate composite sync. The CRT controller chip's (CRT 5037) internal registers are programmed at startup by the application software. In addition, the BUFFER board has several internal registers to control its operation and to Pan/Scroll the diagnostic display.

The BUFFER board has a local processor interface which meets the Motorola MVMX32 bus specification (32-bit high speed bus) and which is compatible with a subset of the standard VSB bus. The BUFFER address locations on this bus are DIP-switch selectable in the range 000000 to FFFFFF hexadecimal on 2 M-byte boundaries. The RAB addresses range from 00000 to FFFFF for MVMX32 read/write accesses while the RIB addresses range from 100000 to 13FFFC for read-only access. The BUFFER board internal registers, as well as the CONVERTER registers, reside in the region 140000 to 1FFFFF. The RAB is written to as a 1K by 1K byte array and read back by the local processor as a 256 by 1K longword (32-bit) array. The RIB is read by the local processor as a 64 by 1K longword array. Neither the RAB nor the RIB support data realignement on non-longword boundaries.

The BUFFER board differs most notably from a conventional memory board in that it is dual ported with the local (MVMX32) bus and the CONVERTER board's proprietary synchronous bus. These two busses are time shared on a 50% duty cycle basis with full handshake and acknowledge for the MVMX32 bus. The diagnostic video display is suspended during those cycles when the local processor is accessing the RAB or RIB. Because of the 50% duty cycle basis of operation, the RAB and RIB provide average access times to the local processor of 800ns/transfer for 0.8 Mbytes/sec writing to the RAB and 3.2 Mbytes/sec reading the RAB or RIB. The MVMX32 protocol tends to increase these access times by up to 50%.

BUFFER BOARD MEMORY AND REGISTER PROGRAMMING INFORMATION

2.2. RAB MEMORY:

2.2.1. READ ACCESS

```
BIT:  3130292827262524232221201918171615141312111009080706050403020100

      [    BYTE 0    ][    BYTE 1    ][    BYTE 2    ][    BYTE 3    ]
```

The above figure shows the logical byte orientation of read data on the MVMX32 bus for a RAB read access. Byte 0 represents the leftmost byte out of each group of four bytes. This is equivalent to the leftmost pixel in a raster scan display and is the same representation used in the diagnostic display. During a read access to the RAB, the two least significant bits (LSb) of the RAB address A0,A1 are don't cares. A Motorola 130-type processor board, following the MVMX and VSB standards, will request additional longword reads if the original read was not on a longword boundary (A0,A1 = 0). All read accesses to the RAB should be explicit longword accesses on longword boundaries.

The actual data received from the RAB during a MVMX32 bus read represents the 8-bit digital data (0-255) either placed in that byte location by the processor (MVMX32 write) or placed there as a result of a polar to cartesian conversion by the CONVERTER board. There is no source information in the data to indicate from which path the data arrived. The RAB can be used for general purpose data and program storage as long as the longword nature of the RAB is maintained. The RAB's compatibility for these purposes should be checked with the user's compilers, assemblers and operating system.

Normal operation of the BUFFER board in a radar sub-system would employ a 512 by 512 byte quadrant of the RAB, leaving the other three quadrants for subsequent radar frame storage or general use. The usual quadrant would be the top left one (QUAD0) starting at location 00000 hex and ending at 7FDFF. The 10 MSb's of the 20 bit RAB address represent the vertical line location (0-1023) of the 1024 by 1024 array. The 10 LSb's of the RAB address represent the horizontal byte location (0-1023). To read the top left quadrant of the RAB, execute 128 longword reads starting at 00000, add 512 to the address counter and then read 128 longwords from the next line of the array. Continue this for 512 lines for a total of 256Kbytes (64K longword reads).

RAB ADDRESS DESIGNATION - X = HORIZONTAL, Y = VERTICAL

A20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

2 LSbits are don't care for RAB READS

The address map for the RAB is shown below (Figure 2.1) :

ADDRESS:

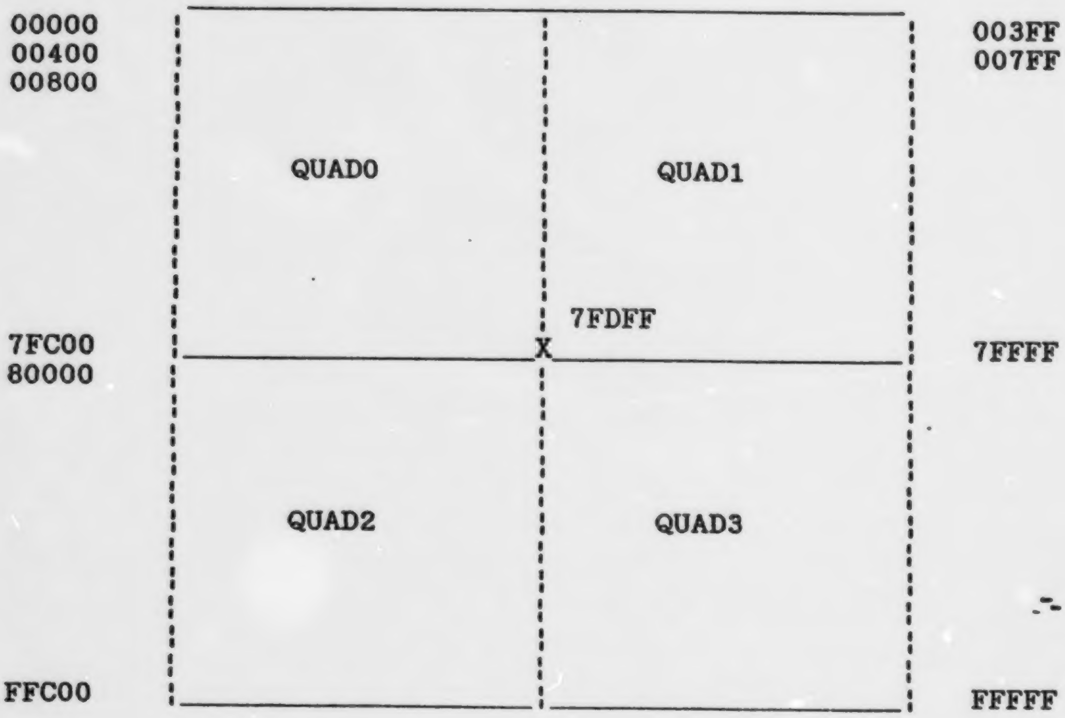

00000
00400
00800
003FF
007FF
QUAD0
QUAD1
7FDFF
7FC00
80000
X
7FFFF
QUAD2
QUAD3
FFC00
FFFFF

Figure 2.1 RAB ADDRESS MAP

2.2.2. WRITE ACCESS

```
BIT:   3130292827262524232221201918171615141312111009080706050403020100

       [    DATA       ][      N/C       ][      N/C       ][    N/C       ]
           8 BITS
```

The above figure shows the logical byte orientation of write data on the MVMX32 bus for a RAB write access. Data to be written to the RAB must be placed in the 8 MSbits of the 32 bit data word. As the RAB always answers back to the local processor as an eight bit slave device on a write access, the local MVMX32 processor will always properly assert the data on the correct data lines. The user can write to the RAB in either longword, word or byte mode.

Normal operation of the BUFFER board in a radar sub-system would require writes to the RAB only to clear (set to 00 hex) it on startup and after range and resolution setting changes. The RAB can be set to 0 by writing bytes of 00 to all the 1M (1024 X 1024) RAB locations or by writing 00000000 to all the 256K longword equivalent addresses. The MVMX32 processor will request four consecutive RAB writes for each longword attempt thereby clearing the RAB in approximately 1/4 as much time as the byte method.

RAB ADDRESS DESIGNATION - X = HORIZONTAL, Y = VERTICAL

A20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

2 LSbits ARE used for RAB BYTE WRITES

the RIB using the ERASE bit in the PAN register and thereafter erase the RIB only when control changes in the CONVERTER indicate the necessity or desireability of doing so.

The RIB memory array uses the same Dynamic Ram memories (DRAMs) as the RAB. There are four 256K by 4 bit SIP memory modules organised as a 256K by 16 bit memory block. Only 2 Mbits of the RIB's total 4 Mbit storage capacity are utilised due to the required function of the RIB and the design of conventional DRAMs. All 8 Mbits capacity of the eight RAB SIP modules are being utilised.

RIB ADDRESS DESIGNATION - X = HORIZONTAL, Y = VERTICAL

A20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	X9	X8	X7	X6	X5	X4	X3	X2

2 LSbits NOT used for RIB READS

The address map for the RIB is shown below (Figure 2.2) :

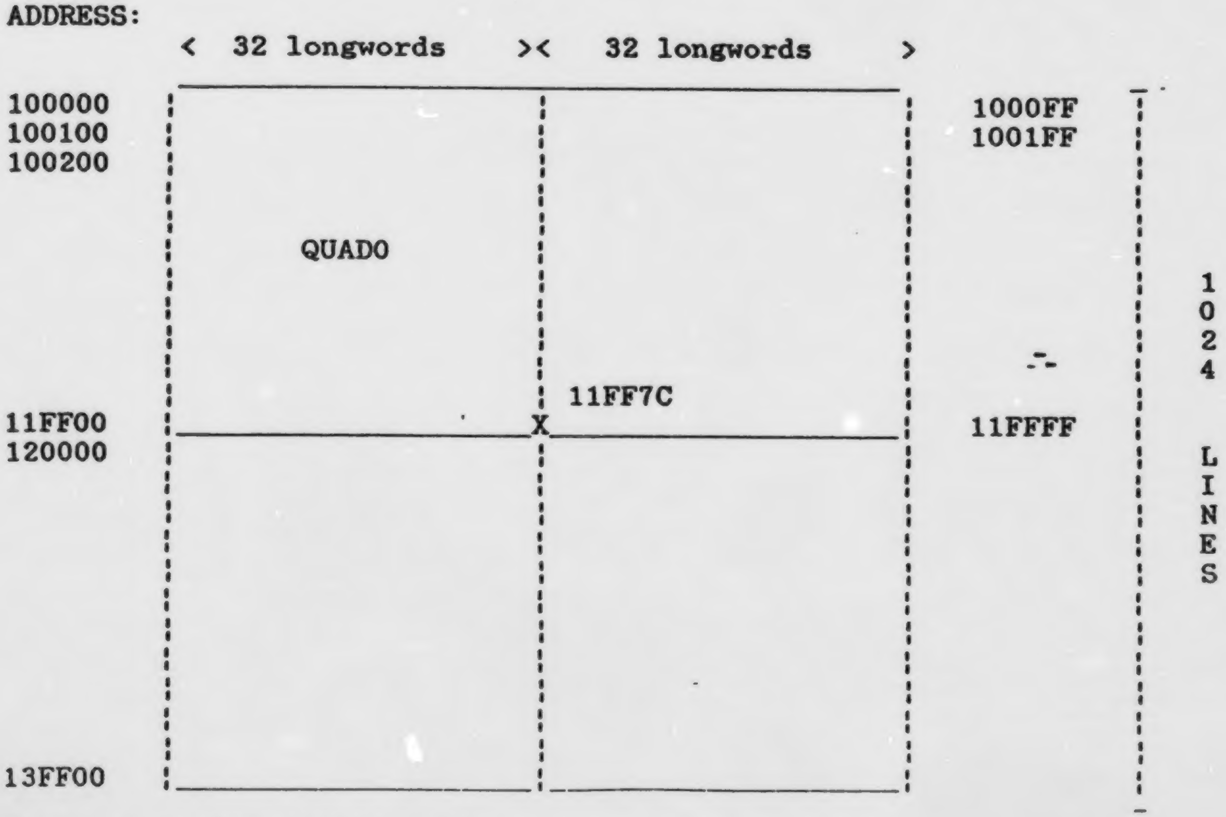

ADDRESS:
< 32 longwords
>< 32 longwords >
100000
100100
100200
QUAD0
11FF7C
X
11FF00
120000
13FF00
1000FF
1001FF
11FFFF
1024 LINES

Figure 2.2 RIB ADDRESS MAP

2.4. CRT CONTROLLER ADDRESS 141000 -14100F

The BUFFER board has an onboard CRT Controller chip (CRT 5037, see data sheet in Appendix) utilised both for diagnostic display generation and for the required DRAM refresh timing. The CRT5037 operates from the onboard hard-wired video and DRAM timing logic which in turn operate from a 20 MHz crystal circuit. Changing this crystal frequency will modify the basic board timing including the critical RAS and CAS timings for the DRAMs. The CRT5037 has internal registers which must be properly configured on power-up before the BUFFER, CONVERTER and DIGITIZER boards can be used. These registers define the timing of the video horizontal and vertical memory addresses as well as the horizontal and vertical retrace signals. These addresses and retrace signals will insure proper DRAM refresh and video display if set according to the programming instructions in this section. While the BUFFER board circuitry has been designed to allow significant variation in the CRT5037 operation, only personnel with a very good understanding of video timing and waveforms should attempt any modification.

The CRT5037 internal registers are located at addresses 141000 to 14100F hex. These are byte write only addresses. Some of the internal registers are not functional and are not included in the setup procedure detailed below. More information can be found in the Appendix.

CRT CONTROLLER STARTUP VALUES AND SEQUENCE

ADDRESS	NAME	SETUP VALUE	FUNCTION
141000	REG0	50 HEX	; HORIZONTAL LINE COUNT
141001	REG1	BF	; INTERLACE & HORIZ. SYNC TIMING
141002	REG2	33	; H. SCANS & CHARACTERS PER ROW
141003	REG3	BF	; SKEW & ROWS PER FRAME
141004	REG4	14	; SCAN LINES PER FRAME
141005	REG5	0E	; VERTICAL DATA START
141006	REG6	3F	; LAST DATA ROW
14100A	RESET	00	; RESET CRT5037
14100E	START	00	; START CRT5037 TIMING CHAIN

SETUP SEQUENCE

```
EXECUTE BYTE WRITE TO    14100E    ; START
                         14100A    ; RESET
                         141000    ; LOAD REG. 0
                         141001    ; LOAD REG. 1
                         141002    ; LOAD REG. 2
                         141003    ; LOAD REG. 3
                         141004    ; LOAD REG. 4
                         141005    ; LOAD REG. 5
                         141006    ; LOAD REG. 6
                         14100E    ; START - CRT5037 WILL NOW OPERATE
```

Diagnostic video display format provided by the above procedure is;

512 by 512 pixels per frame
30 Hz interlaced display
15 KHz horizontal sync rate
Composite or Separate TTL sync
1 Volt p-p (75 ohm term.) video on pedestal

The PAN and SCROLL registers can be programmed separately to move the diagnostic display about the 1024 by 1024 RIB in steps of 8 pixels and 8 lines.

2.5. CONTROL REGISTERS

The BUFFER board has two registers which can be modified under program control to modify operation of the RIB or the diagnostic display. As with the CRT Controller registers, the PAN and SCROLL registers are restricted to BYTE WRITE access only from the MVMX32 bus. The PAN and SCROLL registers are used together to erase the RIB.

2.5.1 PAN REGISTER ADDRESS 141040

BIT	31	30	29	28	27	26	25	24
FUNCTION	[ERASE]	[PAN 6	PAN 5	PAN 4	PAN 3	PAN 2	PAN 1	PAN 0]

When set = 1, the ERASE bit causes a value of 00 to be written to all RIB locations addressed by the diagnostic display and the CONVERTER board. The MVMX32 bus should not access the RIB when ERASE = 1. Only the 512 by 512 area of the RIB currently displayed by the diagnostic display, as controlled by PAN and SCROLL, will be cleared. The RIB will continue to be cleared until ERASE = 0. The ERASE bit should be set to 1 for at least one complete frame time. For a 30 Hz interlace display, this time equals 1/30 sec. or 34 milliseconds. To erase only QUAD0 of the RIB, set PAN 0-6 to 0000000 and SCROLL 0-5 to 000000. The pan and scroll values are used to define the top left corner of the RIB window to be erased. The ERASE bit can only function if the CRT controller has been setup and is operating correctly.

The value contained in bits PAN 1-6 define the amount of right shift, in steps of 8 pixels, that is applied to the diagnostic display. The display can be shifted from 0 - 512 pixels allowing the entire horizontal extent of the RIB to be seen. These bits do not affect the CONVERTER operation.

2.5.2 SCROLL REGISTER ADDRESS 141044

BIT	31	30	29	28	27	26	25	24
FUNCTION	[BIT CONTROL]		[SCROLL]					
	1	0	5	4	3	2	1	0

The value contained in bits SCROLL 0-5 define the amount of down shift, in steps of 8 lines, that is applied to the diagnostic display. The display can be shifted from 0 - 512 lines allowing the entire vertical extent of the RIB to be seen. These bits do not affect the CONVERTER operation. As noted above in the PAN section, SCROLL 0-5 define the RIB window to be erased when ERASE = 1. The table below indicates appropriate values for the four standard quadrants.

QUADRANT	PAN	SCROLL
0	00	00
1	40	00
2	00	20
3	40	20

POWERUP RIB ERASE SEQUENCE (FOLLOWS CRT5037 SETUP)

WRITE TO REG.	DATA	PURPOSE
PAN	80	; QUAD0 & ERASE
SCROLL	00	; QUAD0
- WAIT 34 msec -		; LET QUAD0 ERASE
PAN	C0	; QUAD1 & ERASE
SCROLL	00	; QUAD1
- WAIT 34 msec -		; LET QUAD1 ERASE
PAN	80	; QUAD2 & ERASE
SCROLL	20	; QUAD2
- WAIT 34 msec -		; LET QUAD2 ERASE
PAN	C0	; QUAD3 & ERASE
SCROLL	20	; QUAD3
- WAIT 34 msec -		; LET QUAD3 ERASE
PAN	00	; QUAD0
SCROLL	00	; QUAD0
		; ERASE OFF

RIB NOW DISPLAYING QUADRANT 0

The two bits BIT CONTROL 0,1 determine which 2 bits of the 8 bit RAB data will be written into the RIB. If the data from the DIGITIZER and CONVERTER boards are normalized to the full 8 bit dynamic range, for example, it would be possible using BIT CONTROL 0,1 to select the 2 MSbits of the RAB data and therefore store the peak values in the RIB. The 2 bits selected are contiguous and therefore form a set of 4 possible inputs to the RIB as shown below. Note that BIT CONTROL 0 and 1 only function on CONVERTER accesses to the RIB.

BIT CONTROL		SELECT RAB DATA BITS							
		MSb							LSb
1	0	7	6	5	4	3	2	1	0
0	0							X	X
0	1					X	X		
1	0			X	X				
1	1	X	X						

3. CONVERTER BOARD DOCUMENTATION:

The Converter board is responsible for performing the polar to cartesian conversion of radar data and then placing the data in the Buffer board in a raster scan format. The Converter board receives the radar data from the Digitiser board and then processes the data, according to internal registers, before passing it on to the Buffer. The Converter is interfaced to the local MVME-130 processor on the MVMX32 bus and is programmed by accessing its internal registers which are preset to unused memory locations. All Converter register and memory locations are 16 bit data words for read or write access. The Converter can also supply, if enabled, a MVMX32 interrupt request signifying the start of a new polar to cartesian conversion.

The programmable Converter registers are;

REGISTER	BASE ADDRESS	FORMAT	MODE	R/W
STC	140000-1403FE	512 X 2 X 8 BIT	WORD	W
OFFSET	140800	16 BIT	WORD	W
XSTART	140804	"	"	W
YSTART	140808	"	"	W
CONTROL	14080C	"	"	W
AZIMUTH	140810	"	"	R
PRF	140814	"	"	R
PROCESS	140818	"	"	W
COSINE	140820	"	"	W
SINE	140824	"	"	W
CNTRLRD	140828	"	"	R

NOTE: Address bits 21, 22, 23 are DIP switch selectable. Address bits 24 through 31 must be 0.

3.1. STC REGISTER:

The STC register is organised as 1024 8-bit bytes located in 256 by 4 static random access memories (SRAMs) on the Converter board. These RAMs (type 93422) are high speed (35 nanosec access) memory devices which can be used to modify the input radar signal at the maximum 20 MHz sampling rate of the Digitiser board. The contents of the STC memory will normally be used to provide a range dependent gain function and/or a d.c. level attenuation (gain) to the radar video signal. This memory can be used, however, to apply any analog function to the Digitiser's signal source. The STC is organised as 512 16-bit words, each word containing 2 8-bit bytes left justified. The programmer should set all 1024 bytes to FF if no STC function is desired. Alternately, the STCLOAD bit may be set = 1 with DIGITIZER ON which presents a high-Z (FF) STC to the D/A converter. The STC is set as follows;

1) select STCLOAD and DIGITISER-OFF (see CONTROL reg.)
2) load STC memory (512 word writes)
3) deselect STCLOAD and select DIGITISER-ON
4) select STC sampling rate using STC-SPEED (CONTROL reg.)

3.2 OFFSET REGISTER:

The Offset register is used to apply a rotational offset to the Converter circuitry so that the cartesian image in the Buffer board may be turned relative to any reference location such as north or ship's head. The effect of changing the Offset value from 0 is to change the digital angle which addresses the internal EPROMs which in turn supply the appropriate sine and cosine values for the polar to cartesian conversion. The Offset register also contains a 3-bit RANGE selection word which addresses the same EPROMs and determines which resolution for sine and cosine should be used.

```
 15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

<  RANGE   ><  N/C    ><              OFFSET ANGLE              >
 2   1   0
                        <  0-1023 VALUE,  1 bit = 360/1024 deg>
```

RANGE 2 1 0	RESOLUTION X NORMALISED SINE, COSINE
0 0 0	1.00
0 0 1	0.75
0 1 0	0.50
0 1 1	0.25
1 0 0	0.6933
1 0 1	0.3466
1 1 0	0.2766
1 1 1	0.1733

The last four (RANGE 4 - 7) resolution values were programmed into the EPROMs to allow the Converter to produce the same display ranges as the Sperry MK-16 and MK-127 radars. The appropriate RANGE and DIGITISING SPEED SETTINGS are as follows;

DESIRED RANGE (nautical miles)	RANGE 0-2	DIGITISING SPEED (MHz)	ZOOM
0.259	000	20.0	4X
0.75	101	"	4X
1.50	100	"	1X
3.00	101	"	1X
6.00	101	10.0	1X
12.00	101	5.0	1X
24.00	101	2.5	1X
60.00	110	1.25	1X
120.00	110	0.625	1X

3.3 XSTART, YSTART REGISTERS:

The XSTART and YSTART registers are each 10 bit values (0-1023) used to position the beginning of each radar radial or line drawn. These registers allow the programmer to place the radar image anywhere inside the 1024 by 1024 buffer memories of the Buffer board. The radar data is normally converted into a 512 by 512 area, so a starting X,Y of 255,255 (XSTART=FF, YSTART=FF) would center the cartesian radar image in the top left quadrant of the Buffer. The XSTART and YSTART registers should be updated on an interrupt basis (see CONTROL register) to ensure that the X and Y addresses are not changed while a line is being drawn. Figure 3.1 shows examples of XSTART and YSTART values.

```
 15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

<      N/C              ><      10 bit XSTART or YSTART         >
```

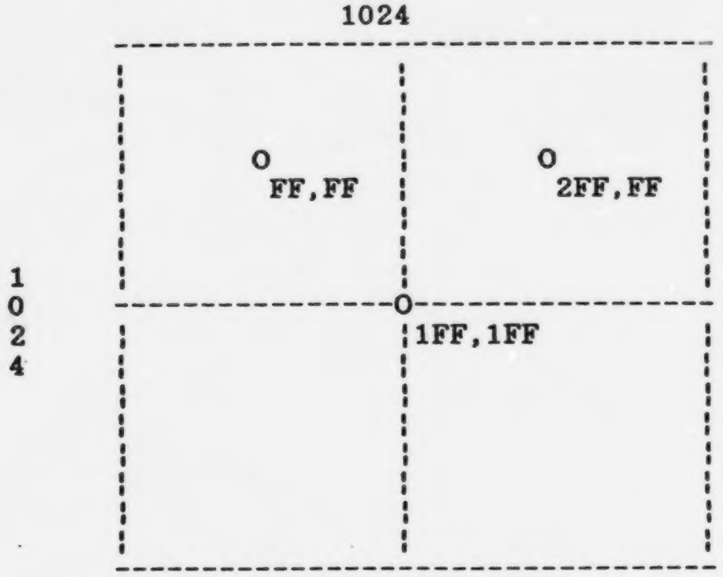


Figure 3.1 Example XSTART and YSTART values

3.4 CONTROL REGISTER:

The CONTROL register contains most of the control bits affecting the timing of the Converter board. Refer to the PROCESS register for the signal processing and other control bits. The CONTROL register also affects the Digitiser and STC sampling rates. The register bits are arranged as follows;

```
    15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

   <  LENGTH  > N/C  ¦   ¦ N/C  ¦   ¦   ¦  <  DIG    > <  STC    >
    2   1   0        ¦   ¦      ¦   ¦   ¦    SPEED        SPEED
                     ¦   ¦      ¦   ¦   ¦
                     ¦   ¦      ¦   ¦   ¦______ DIGITISER ON/*OFF
                     ¦   ¦      ¦   ¦
     STCLOAD ________¦   ¦      ¦   ¦__________ MVMX32 INT. ENABLE
                         ¦      ¦
  LATCH/*EPROM __________¦      ¦______________ *CLEAR CONVERTER
```

3.4.1. LENGTH 0-2 : This three bit register instructs the Digitiser board to sample either 1024, 512 or 256 range bins. The LENGTH 2 bit is held high to limit the Digitiser to 1024 samples. The LENGTH 1 (512 samples) and LENGTH 0 (256 samples) bits may need to be set when the slowest digitising rates are used to enable digitising and scan conversion with high antenna rotation rates. This is generally not a problem with radar systems as the antenna rate should be lower for longer range transmitters with their lower pulse repitition frequencies (PRF). The programmer should ensure that he is not trying to digitise and convert radar data for a range longer than is possible with the available PRF. A radar system with PRFs of 2000, 1000 and 500 operating with 30 rpm antenna has maximum possible (not necessarily useable) ranges of 75, 150 and 300 Km respectively.

3.4.2. STCLOAD : This bit must be set to 1 (logic high) to modify the STC RAM. The STC RAM output is disabled while STCLOAD is active. The Digitiser should be turned OFF (see DIGITISER ON/*OFF) while modifying the STC.

3.4.3. LATCH/*EPROM : This bit should be set to 0 (logic low) to use the preprogrammed sine and cosine values from the onboard EPROMs for the polar to cartesian conversion. This bit should be set to 1 if the programmer wishes to utilise the SINE and COSINE registers to define the conversion process.

3.4.4. *CLEAR CONVERTER : This bit should be set to 1 for normal operation. It is a diagnostic control which allows the Converter to function under program control when no radar trigger is present. Setting this bit low and then high will cause the Converter to scan convert one line. Toggling this bit at the antenna rotation rate will simulate a working radar.

3.4.5. MVMX32 INT. ENABLE : When set to 1, MVMX32 interrupt requests can be generated by the Converter board. The MVMX32 *IRQ line on the J2 backplane will be driven low coincident with the indication that the antenna has turned to the next allowable position (1024 per 360 degrees) in its rotation. This is equivalent to a low to high transition on the Synchro to Digital Converter's 360 deg./2048 line. The *IRQ bus line will remain active until MVMX32 INT. ENABLE is set to 0 or until a word read is executed at the CNTRLRD (base : 140828) register.

When set to 0, no interrupt requests will occur on the bus. MVMX32 INT. ENABLE is automatically cleared on power-up.

It is suggested that all modification of registers be done in synchronisation with the Converter's interrupt request in order that the Converter operation not be modified while in progress. When the Digitiser is sampling at 20MHz, the maximum guaranteed allowable interrupt latency is 50 micro seconds. The alternative to interrupt service is to turn the Digitiser OFF while Converter registers are modified.

3.4.6. DIGITISER ON/*OFF : Set to 1 = ON, set to 0 = OFF

When the Digitiser is OFF, the Converter continues normal operation with the exception that it will not modify the Buffer memories.

3.4.7. DIGITISER SPEED : Sets the Digitiser sampling rate in relation to the Digitiser's onboard oscillator as follows;

OSCILLATOR SPEED	BITS			SAMPLING RATE (MHz)	MAXIMUM RANGE Km/Nm
	2	1	0		
40 MHz	0	0	0	20.00	7.6/4.2
	0	0	1	10.00	15.3/8.5
	0	1	0	5.00	30/17
	0	1	1	2.50	61/34
	1	0	0	1.25	122/68
	1	0	1	.625	245/136
	1	1	0	.3125	491/273 **
	1	1	1	.15625	983/546 **

** These values not useful for conventional marine radar

3.4.8. STC SPEED : Sets the STC correction sampling rate of the STC RAM in relation to the Digitiser's onboard oscillator as follows;

OSCILLATOR SPEED	BITS 2	1	0	SAMPLING RATE (MHz)	MAXIMUM RANGE Km/Nm
40 MHz	0	0	0	20.00	7.6/4.2
	0	0	1	10.00	15.3/8.5
	0	1	0	5.00	30/17
	0	1	1	2.50	61/34
	1	0	0	1.25	122/68
	1	0	1	.625	245/136
	1	1	0	.3125	491/273 **
	1	1	1	.15625	983/546 **

** These values not useful for conventional marine radar

The STC sampling rate is independent of the Digitiser sampling rate. It is therefore possible to fill the STC RAM with the desired waveform for a medium or long range and set the sampling rate accordingly, regardless of the Digitiser rate. The programmer can utilise this capability to reduce the number of STC data changes when the Digitising rate is changed often. If this method of operation is used, the probability of quantizing errors will increase.

3.5. AZIMUTH REGISTER :

The AZIMUTH register is a word read only register which supplies the current pointing position of the radar antenna as determined by the Synchro to Digital board as well as the interrupt status and some control bits. The antenna pointing data represents the 12 most significant bits of the 12-16 bit output of the S/D converter. Each bit represents 1/4096 of 360 degrees rotation. Refer to the description of the Synchro to Digital Converter board. The IRQ bit will be 1 when there is an interrupt enabled and pending. The LENGTH 0-2 bits reflect the actual onboard value of the LENGTH word set in the CONTROL register.

```
 15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

<  LENGTH ><IRQ><    12-bit ANTENNA AZIMUTH    0 - 4095       >
 2   1   0
```

3.6. PRF REGISTER :

The PRF register (16 bit read only) supplies a measured elapsed time value representing the interval between radar pulses which can be used to differentiate between the several pulse repitition frequencies (prf) available in a radar set. Although the time value is not exact, it is sufficiently different for the constant PRFs that the programmer can set up a table for comparison purposes. The onboard timebase oscillator can be changed for differing applications by varying the values of R10 and C8. These two components define an RC time constant. The PRF register also supplies status bits which show the state of some of the CONTROL register bits.

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

 ¦   ¦  <DIG SPEED> <STC SPEED> <    8 bit  PRF COUNT        >
 ¦   ¦
 ¦   ¦______ DIGITISER ON/*OFF          PRF        COUNT (APPROX)
 ¦__________ DIGITISER AVERAGE         4000            1
                                       2000            8
                                        400           25
```

3.7. PROCESS REGISTER :

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0

     *   *
D    Z   Z   T   C   B   B   B   P   P   F   A  <T3  T2  T1  T0>
I    O   O   E   L   U   U   U   5   2   T   D
G    O   O   S   E   F   F   F   1   5   C   A
     M   M   T   A   F   F   F   2   6       P
A                R   E   E   E               T
V    8   4           R   R   R
E    X   X                                   T
R                    A   M   M               H
A                    V   A   I               R
G                    R   X   N               S
E                    G                       D
```

3.7.1. DIGITISER AVERAGE - = 1 selects radial averaging (4 radials) in the high speed Digitiser memory. Causes four consecutive radar pulse returns to be added together and then finally shifted right 2 bits and sent to the Converter at the end of the fourth radial. This function should only be selected when the radar set can supply 4 complete pulses for each of the 1024 azimuths per rotation (ie short range , PRF = 2000, for 30 rpm MK 127). This function significantly reduces cross range noise and clutter.

3.7.2. *8X , *4X ZOOM - Active low controls which cause the Converter to draw each radar point either 4 or 8 times at the current sine, cosine and resolution rates. Should not be used together for 12X ZOOM. Normally, both are set to 1 (high) for a zoom factor of 1. Note that a zoom of 4 takes 4 times as long to write a line into the Buffer as a zoom of 1.

3.7.3. TEST - When = 1, forces a test pattern, which is a count from 0-255,0-255,0-255,0-255, to be used in place of the Digitiser data. Overrides all control bits except CLEAR.

3.7.4. CLEAR - When = 1, forces the Converter to write 00 at all addressed locations in the Buffer. Overrides all control bits.

3.7.5. BUFFER AVERAGE - When = 1, the Converter will average the results of other onboard processing with the current contents of the addressed location in the Buffer board (RAB). The averaged data is then written to the Buffer's RAB and RIB. Overrides MAX and MIN.

3.7.6. BUFFER MAX, BUFFER MIN - When = 1, causes the Converter to compare the results of onboard processing to the addressed Buffer location and then write the maximum (MAX) or minimum (MIN) of the two back into the Buffer.

3.7.7. P512 , P256 - When = 1, these bits, respectively, cause the Converter to convert only 512 or 256 radar points instead of 1024 before terminating the radial conversion. While the Converter will not write outside of the Buffer's 1024 by 1024 window, it will cross from one 512 by 512 quadrant to another. It is possible to restrict the Converter to one quadrant using these bits although it is usually necessary to place the radar at the center of a quadrant. Note that you should not try to convert more radar points than you have digitised and so these bits are tied to the CONTROL registers LENGTH control.

3.7.8. FTC - When =1, instructs the Converter to apply the fast time constant (FTC) filtering to the input data from the Digitiser. The FTC is a running three sample average along the radial which is used to remove high frequency components (noise, sea clutter etc..) from the radar data. FTC can be used only when ADAPTIVE THRESHOLD = 1 and it then turns ADAPTIVE THRESHOLD OFF. The gain function T0-3 can be used to move the resultant filtered values up in amplitude.

3.7.9. ADAPTIVE THRESHOLD - When =1, instructs the Converter to apply the adaptive thresholding filter (ATF) to the incoming Digitiser data. The ATF detects rising edges (increases) between consecutive data samples and allows only the arithmetic difference to pass through to the Buffer. Bits T0-3 act as gain on the ATF data. Because the ATF passes only the difference between samples, it may be necessary to process lower order data bits for such tasks as target detection and radar-coastline correlation. ATF transforms resulting radar images into thin line representations of all targets' leading edges. The noise, clutter, rain and snow removal ability of ATF is very much less effective with linear radar amplifiers. The ATF bit must be set to 1 for FTC to function, in which case ATF is not functional.

3.7.10. T0-3 - When ADAPTIVE THRESHOLD = 1, T0-3 act as a 4-bit additive gain on the resultant ATF or FTC data values.

3.8. COSINE, SINE REGISTERS

The Converter has been equipped with two 16 bit registers which can be used to supply the sine and cosine values manually. These registers allow a much greater number of transforms than do the pre-programmed EPROMs which can supply only the eight resolutions for the standard polar to cartesian conversion.

Each of the COSINE and SINE registers can supply 15 bits of normalised (0 - 32767) sine or cosine values (representing the possible values of 0.0000 to 1.0000 for the angles 0 - 90 degrees) along with a sign bit (MSbit) for drawing lines in any direction. The sign bit is relative to the typical raster scan array format of increasing X to the right and increasing Y down. These registers would normally be updated before the Converter starts to draw a new line. This synchronisation can be accomplished by utilising the interrupt request function on the Converter board (see CONTROL register). The maximum interrupt latency time for trouble free operation is 50 micro-seconds.

These registers can be used for, among other things, the transform of polar to B-scan conversion whereby each radar radial is drawn as a horizontal line at consecutive vertical positions in the Buffer memory. To implement this type of transform, set XSTART = 0, YSTART = 0, SINE = 7FFF, COSINE = 0000 and then increment YSTART at each new radial interrupt. These settings will fill the 1024 by 1024 Buffer memory with the 1024 radials of 1024 samples. Various versions of this or any other transform may be developed and then used under interrupt control or implemented by reprogramming the onboard EPROMS.

SINE REGISTER :

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

<SIGN>< 15 bit Normalized Sine - 0000 to 7FFF >

SIN(0) = 0000, SIN(90) = 7FFF, SIN(270) = FFFF

COSINE REGISTER :

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

<SIGN>< 15 bit Normalized Cosine - 0000 to 7FFF >

COS(0) = FFFF, COS(90) = 0000, COS(180) = 7FFF

3.9. CNTRLREAD REGISTER :

A word read operation at this register location will clear any MVMX32 interrupt generated by the Converter. The Converter can only cause an interrupt (*MIRQ = 0) if the INTERRUPT ENABLE bit = 1. This register operates in this manner to satisfy the MVMX32 bus interrupt handling sequence which uses a polling scheme to determine the identity of the interrupting device. No data can be read from or written to this register.

4.1 DIGITIZER BOARD OVERVIEW

The DIGITIZER board is designed to digitize an incoming unmodulated radar video signal which is synchronised to the leading edge of its associated radar trigger pulse. The DIGITZER can operate at a maximum guaranteed rate of 20 MHz. The circuit is divided functionally into an analog and a digital section. The analog section contains input video op amps for voltage gain setting, a Digital to Analog converter (DAC) for supply of analog time-varying-gain (TVG, STC), a difference op amp to apply the gain and an Analog to Digital Converter (ADC) to supply the digital data to the digital section of the board. The digital section contains high speed Static Random Access Memories (SRAMs) and high speed averaging circuitry allowing for pulse to pulse averaging of the digital radar data at the maximum 20 MHz sampling rate. The DIGITIZER board uses the standard double Eurocard form factor but does not have its own VME or MVMX32 bus interface. The circuit board uses the 96-pin P1 connector to interface to its companion CONVERTER board. The DIGITIZER passes digital radar data, the radar trigger and some control bits to the CONVERTER. The CONVERTER, in turn, passes digital STC data, SRAM addresses for radar data and control bits (mostly from the CONVERTER's CONTROL register). The DIGITIZER has no direct connection to the BUFFER board. The 96-pin P2 connector is not soldered to the circuit board in order to provide room for the entry of the radar video and trigger cables.

The onboard ADC and DAC are standard high quality TRW (second sourced) components which require only that the power supplies, voltage references and input analog signals fall within the normal operating specifications. NOTE that potentiometers on the board should not be varied without simultaneously verifying the important voltage levels. The user can setup the board in a stage by stage manner, for any custom application, by utilising the inter-stage jumper or solder connections. The rest of the analog components are standard, short delivery, items with the exception of the HARRIS HA1-2539 op amps. Most of the digital components are standard 74 "F" series integrated circuits. A detailed description of the DIGITIZER circuitry is included because, unlike the BUFFER and CONVERTER, it requires setup and tuning for each application.

The current revision level of the DIGITIZER is Revision "1.0" with ECO's applied as per the Appendix.

4.2 Analog Digitizer Section.

4.2.1 Functional Description:

The following figure (Fig. 4.1) shows the important elements of the Analog Section as numbered for the documentation.

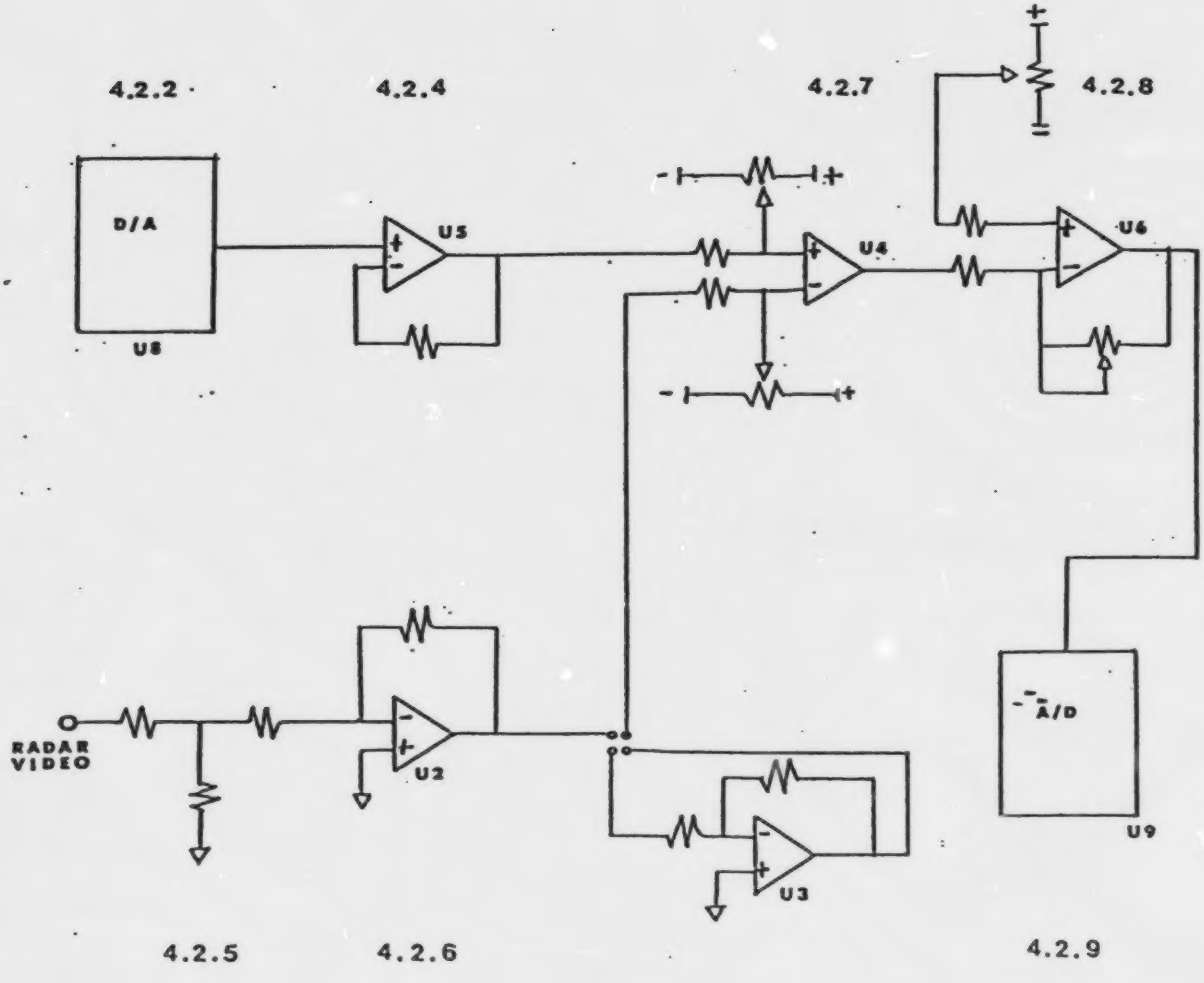

4.2.2
4.2.4
4.2.7
4.2.8
D/A
U8
U5
U4
U6
+
-
RADAR VIDEO
U2
U3
A/D
U9
4.2.5
4.2.6
4.2.9

Figure 4.1 Analog Section

4.2.2 Digital-to-Analog Converter (D/A).

The 8-bit TDC1016 Digital-to-Analog converter develops an output voltage proportional to the value of the STC digital input data, supplied by the Converter Board, and the analog voltage reference. This voltage is applied to the Radar Video as the STC correction.

The rising edge of the STC Clock (STCCLK) pulse transfers STC data from the input lines to the internal 8-bit register. The magnitude of the output voltage is directly proportional to the magnitude of the STC digital input word (i.e. -1 to 0 Volts). The output resistance at this point is about 80 Ohms.

The Digital Ground and Analog Ground are returned to the system power supply ground by way of seperate conductive paths to prevent digital ground noise from disturbing the analog circuitry.

The reference input (VREF) of the TDC1016 is set to -1 Volt with respect to the Analog Ground (AGND). Adjusting this voltage is equivalent to adjusting the TDC1016 D/A converter gain. This voltage should be setup initially with circuitry at operating temperature and with the digitizer board in its normal chassis location.

The LM113 Zener Diode (D1) is used to limit the voltage difference between the reference input (VREF) and the analog ground (AGND) from exceeding the maximum permittable voltage difference between them, before the TDC1016 Digital-to-Analog Converter will be damaged.

The minimum and maximum analog output values of the D/A can be checked by jumpering NFL or NFH respectively to digital ground. If both NFH and NFL are connected to ground, the D/A will invert the analog output. See TRW data catalog p. F14 for further explanation. The minimum and maximum output of the D/A should be checked before connecting subsequent stages.

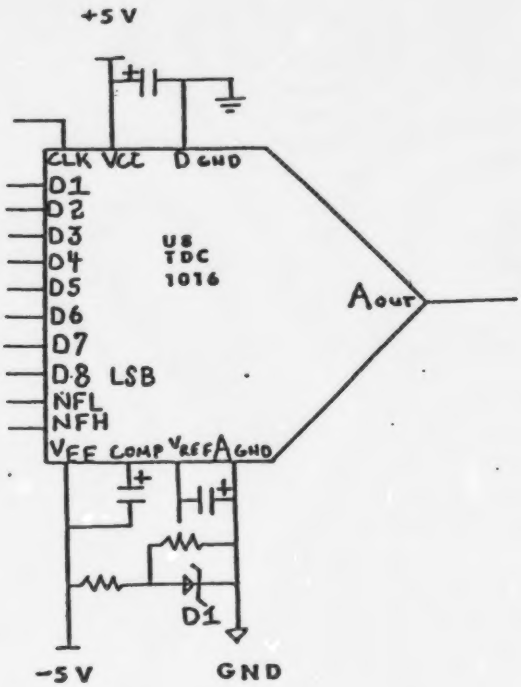

+5V
CLK
VCC
D GND
D1
D2
D3
D4
D5
D6
D7
D8 LSB
NFL
NFH
VEE
COMP
VREF
A GND
U8
TDC
1016
Aout
D1
-5V
GND

Figure 4.2 The TDC1016 Digital-to-Analog Converter

4.2.3 HA-2539 operational amplifier.

The use of the HA-2539 operational amplifier is due to the fact that it is a precision high speed operational amplifier design for applications requiring wide bandwidth and high slew rate. It provides greater stability and ease of use than discrete transistor equivalents. The HA-2539 can also be used to drive low impedance inputs on devices such as the TDC-1048 A/D.

In the design, we needed a high slew rate to process the high frequency signal (20MHz) of the Radar video and STC signal. The maximum frequency signal is 47.745 MHz per stage before deterioration occures.

The slew rate of the operational amplifier HA-2539 is specified to be 600 V/microsec and its maximum rate output is 2 volt, then the full power frequency (fm) will be

$$fm = \frac{SR}{2\pi V} = \frac{600 * 10E6}{(2\pi)(2)}$$

$$= 47.745 \text{ MHz}$$

This is the voltage swing that the operational amplifier can produce without signal distortion (at frequency lower than fm).

When installing the digitizer with a particular radar video source, each operational amplifier stage should be checked for proper response before finally connecting to the A/D.

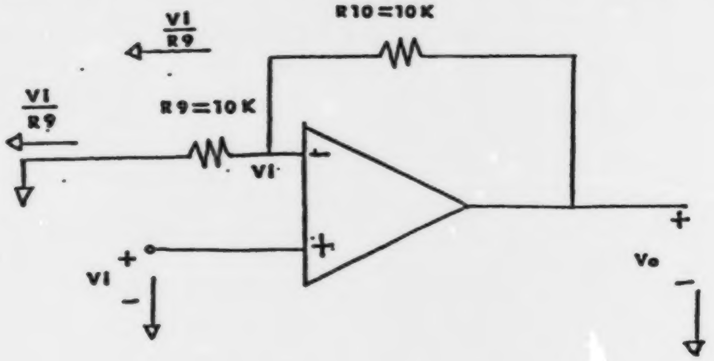
4.2.4. The STC Gain Control (U5).

The gain control is used to optimize the STC signal to match the Radar video signal for range dependent gain applied at the subtractor section. We needed a voltage of -2V to 0V STC radar signal at the input of the subtractor. Therefore we needed to convert the STC signal from (-1V to 0V) to (-2V to 0V).

A noninverting operational amplifier is used . The gain of the noninverting amplifier is

$$\frac{Vo}{Vi} = 1 + \frac{R16}{R19} = 1 + \frac{2k}{2k} = 2$$

This result can be easily verified by analyzing the non-inverting circuit directly. Details of the analysis are shown in Figure 4.3. Note that a virtual short ground exists between the two input terminals; hence the voltage at the inverting terminal is equal to Vi.



$$Vo = Vi + \frac{Vi}{R19}\ R16 = Vi\left(1 + \frac{R16}{R19}\right) = 2\ Vi$$

Figure 4.3. The gain control circuit of STC signal

Input Bias Current is a dc problem encountered in op amps. Fortunately, a technique exists for reducing the value of the output dc voltage due to the input bias current. The method consists of introducing a resistance R21 in series with the non-inverting input terminal. The appropriate value R21 is given by

$$R21 = \frac{R19\ R16}{R19 + R16}$$

therefore, $R21 = \frac{2k * 2k}{(2k + 2k)} = 1\text{kOhms}$

4.2.5 The Input Scaling and Input Impedance Matching.

The Radar video input signal should have a range from positive (or negative) 0 to 10 Volts; and an input impedance of 50 to 1000 Ohms. Different resistor values are selected for different scaling and impedance matching. The scaling resistor is used to provide a 1 Volts Radar video signal to the first op amp stage. The following Input Resistor Selection Table is used.

Input Resistor Selection (values in Ohms)

Zin	1V		2V		4V		5V		10V	
	R2	R1	R2	R1	R2	R1	R2	R1	R2	R1
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	open	499	1k	750	332	806	249	909	110

For input voltages and input impedances which were not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R2 and R1:

$$R1 = \frac{1}{\frac{VR}{Zin} + \frac{1}{1000}} \quad \text{and} \quad R2 = Zin - \frac{1000\ R1}{R1 + 1000}$$

Where VR is the desired input voltage range of the board, Zin is the desired input impedance of the board, and the constant value 1000 Ohms is given by the value of R3.

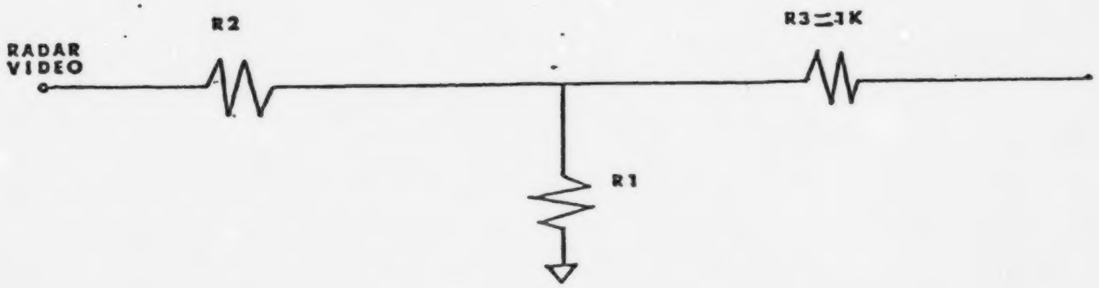


Figure 4.4. The Input Scaling and Input Matching Impedance

After analysing the circuit in Figure 10-43 of the MK-127 Radar Service Manual, the appropriate non-IF (Intermediate Frequency) Radar Video source has been located on the video pre-amplifier pcb connector at RV851 (variable resistor 851). As all gain, STC and FTC are supplied by Sperry in the IF section, a special radar setup and operation sequence will have to be followed. The MK-16 has a similar video pick off point. At RV851, it is necessary to be very sensitive with the Input Impedance Matching and the Input Scaling factors; otherwise the system performance may be degraded due to reflections and ringing in the coaxial cable.

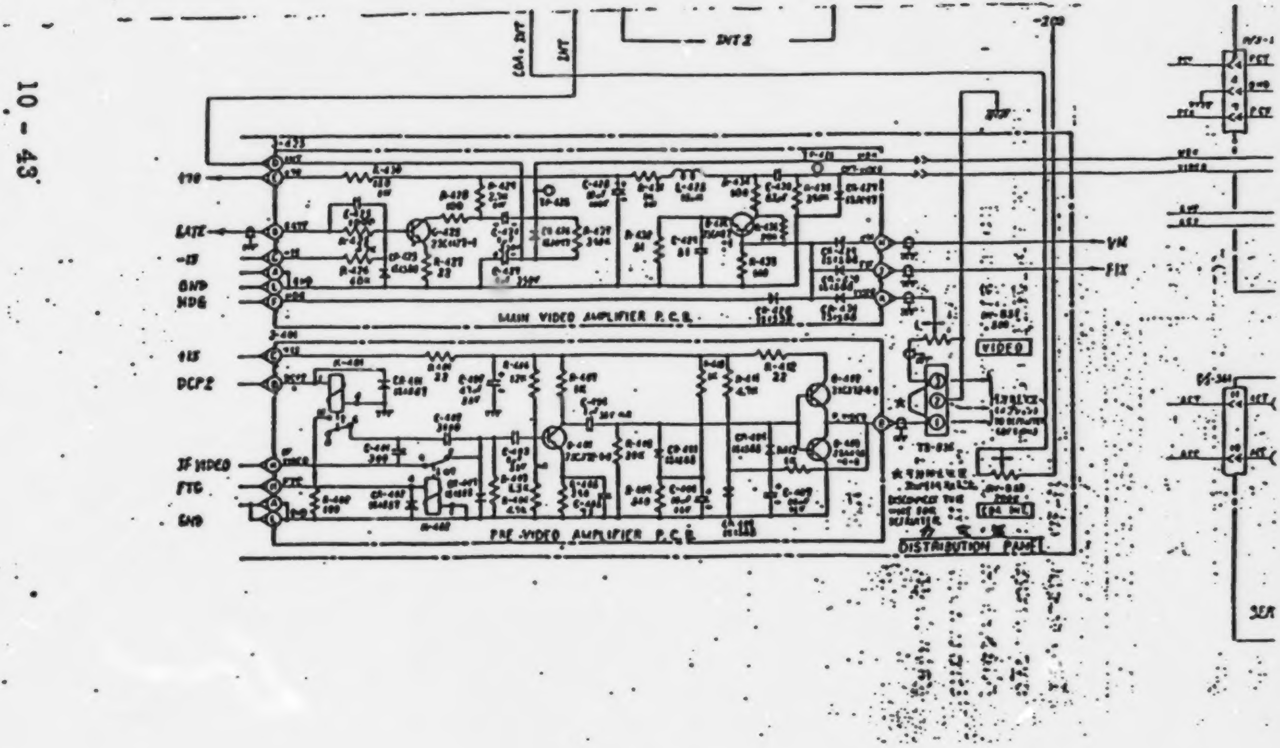
The range of the Video voltage, at this point, is from 0.7 Volts to 14.3 Volts peak to peak.

The following Zin formula is to be used in order to determine the R2 and R1 resistance values in the previous equations,

$$Zin = \frac{1}{\frac{1}{R} + \frac{1}{(500-R) + 1000}} + 100$$

where R is the value between pin 1 and pin 2 of RV-851
in the MK-127 Radar circuit.

For a MK-127 impedance of 100 Ohms and 5 Volts signal at RV-851 the values of R2 and R1 should be 40 Ohms and 10 Ohms respectively, taking into effect a damping resistor at the radar end of the coaxial cable connected to the digitiser board.


10 - 43
INT 2
INT
COM. INT
-200
GATE
-15
GND
HDG
+15
DCP2
IF VIDEO
FTC
GND
VM
FIX
MAIN VIDEO AMPLIFIER P.C.B.
PRE VIDEO AMPLIFIER P.C.B.
VIDEO
DISTRIBUTION PANEL

MK-127 - Figure 10-43 Display Unit of Radar Service Manual

4.2.6 The Radar Video Gain Control (U2).

The gain control is used to optimize the Radar video signal to match the STC radar signal for range dependent gain applied at the subtractor section. We needed the Radar video voltage in the range of -2V to 0V at the input of the subtractor.

Therefore, we need to convert the Radar video signal from the maximum 1 Volt signal level to the range of -2V to 0V level.

To achieved this an inverting amplifier is used. The gain of the inverting amplifier is

$$\frac{Vo}{Vi} = - \frac{R6}{R3}$$

$$= - \frac{2k}{1k} = - 2$$

If the signal is not the desired polarity, another inverting amplifier is to be used to obtain the correct polarity (U3). However, if we have obtained the desired polarity then this section will be bypassed with a jumper to the subtractor section.

The 1.0kOhms resistance value is used to reduce any dc input bias current. This is explained in the STC Gain Control Section.

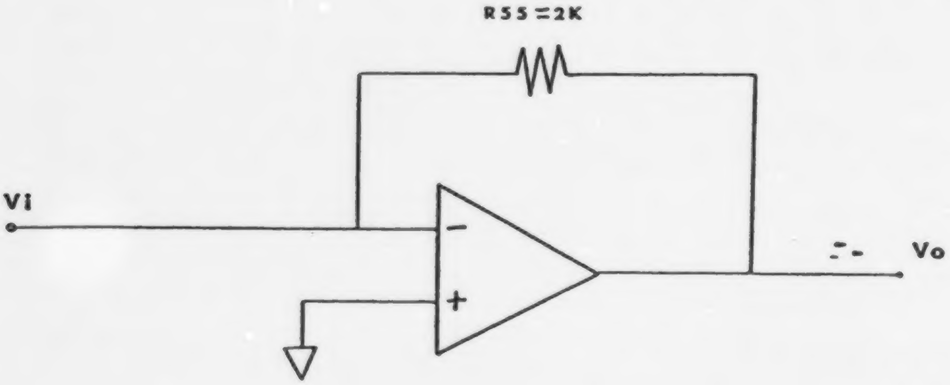
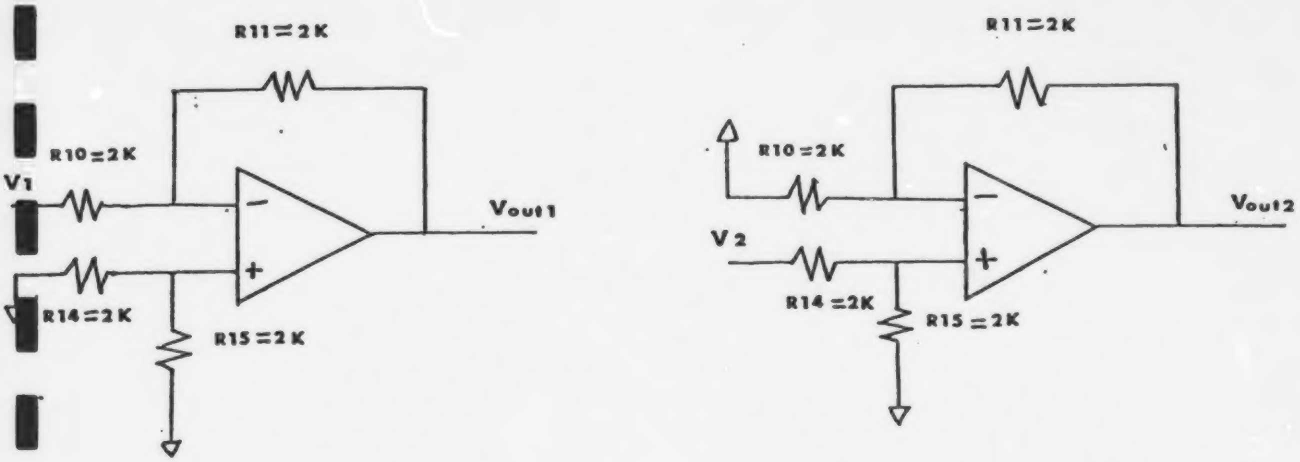


Figure 4.5. The Gain Control Inverting Amplifier

4.2.7 The Subtractor Section (U4).

The STC and the Radar video signals are subtracted to process the desired signal to the A/D converter. In order to achieve this, a difference amplifier is needed. The principle of superposition is used to analyse the following difference amplifier circuit:



6a 6b

Figure 4.6. Application of superposition for analysis

To apply superposition we first reduce V2 to zero : that is, ground the terminal to which V2 is applied. Then we find the corresponding output voltage, which will be due entirely to V1. We denote this output voltage to be Vout1. Its value may be found from the circuit in Fig. 4.6a, which we recognize as that of the inverting configuration. The existence of R11 and R14 does not affect the gain expression, since no current flows through either of them. Thus

$$\mathrm{Vout1} = -\frac{\mathrm{R11}}{\mathrm{R10}}\,\mathrm{V1}$$

Next, we reduce V1 to zero and evaluate the corresponding output voltage Vout2. The circuit will now take the form shown in Fig. 4.6b., which we recognize as the noninverting configuration with an additional voltage divider, made up of R15 and R14, connected across the input V2. The output voltage Vout2 is given by

$$Vout2 = V2 \frac{R14}{R14 + R15} \left(1 + \frac{R11}{R10} \right)$$

The superposition principle tells us that the output voltage Vout is equal to the sum of Vout1 and Vout2. Thus we have

$$Vout = - \frac{R11}{R10} V1 + \frac{(1 + R11/R10)}{(1 + R15/R14)} V2$$

Setting the condition that $\frac{R11}{R10} = \frac{R15}{R14}$

Substituting this result in the output voltage, we have

$$Vout = \frac{R11}{R10} (V2 - V1)$$

which is clearly that of a differential amplifier with a gain of R11/R10.

In the design, we have selected R10 = R11 = R14 = R15 = 2.0kOhms to give

Vout = V2 - V1 i.e. a unity gain.

V1 is the Radar return signal (0 to -2 volts) from stage 6.
V2 is the STC signal (0 to -2 volts) from stage 4.

Vout is the resultant Radar Video including offset and gain as determined by the digital STC. Vout should represent as closely as possible a normalized Radar Video and so U4 should be setup as a non-unity gain amplifier by setting R10 to R15 to provide sufficient gain to fill the dynamic range of the A/D converter i.e. 0 to -2 volts. This is closely coupled to the digital STC and the particular radar receiver being used.

4.2.8 The Fine Tuning Control (U6).

The Fine Tuning Control is used to optimize the signal for the input at the A/D converter (TDC1048). A DC Offset performs the task. The following differential amplifier circuit (Fig. 4.7a) is used:

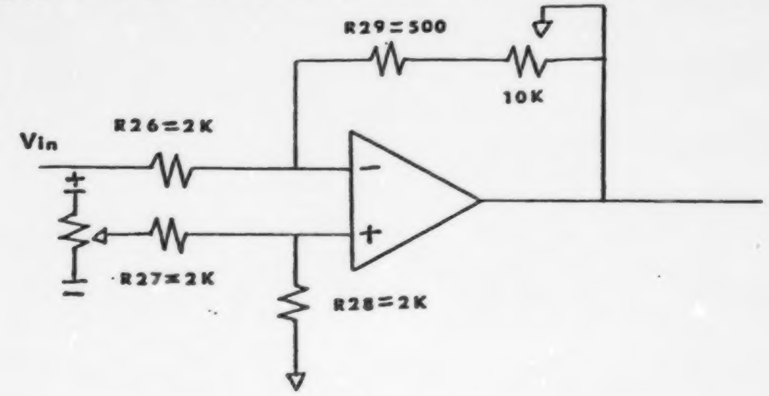

R29=500
10K
Vin
R26=2K
+
−
R27=2K
R28=2K

Figure 4.7a

This circuit is equivalent to Fig. 4.7b

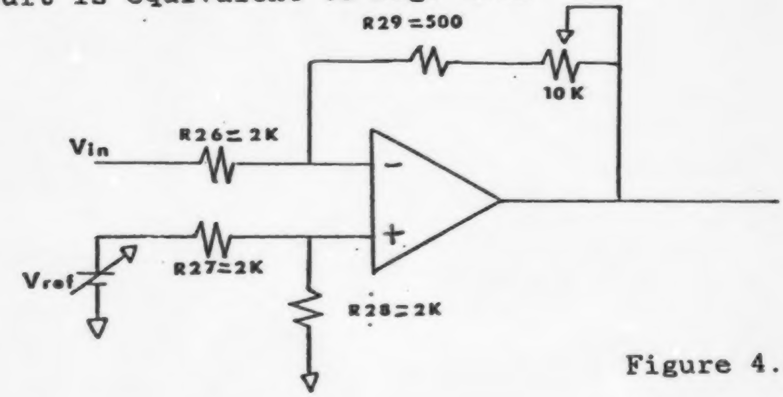

R29=500
10K
Vin
R26=2K
Vref
R27=2K
R28=2K

Figure 4.7b

Analysis of the circuit:

By superposition, we determine the output voltage (Vout). First we ground the reference voltage (Vref), then we have the following circuit (Fig. 4.7c):

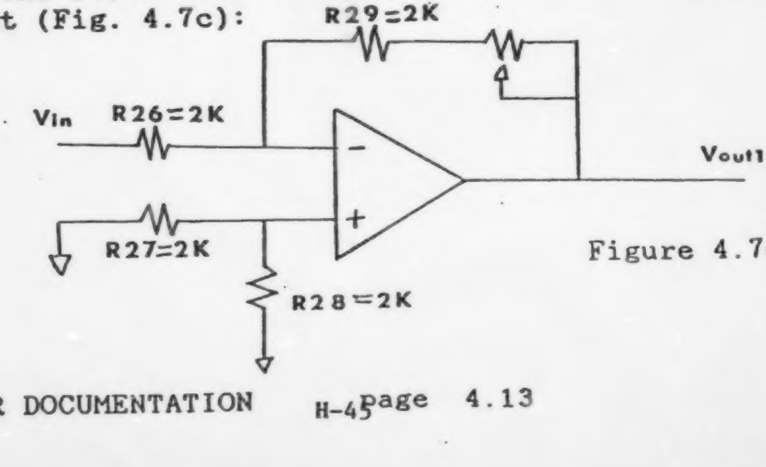

R29=2K
Vin
R26=2K
Vout1
R27=2K
R28=2K

Figure 4.7c

The output is simply, $Vout1 = Vin \; -\frac{R28}{R27}$

$$= Vin \; -\frac{2.0k}{2.0k}$$

$$= - Vin$$

Now we ground the input voltage (Vin), we have the following circuit (Fig. 4.7d):

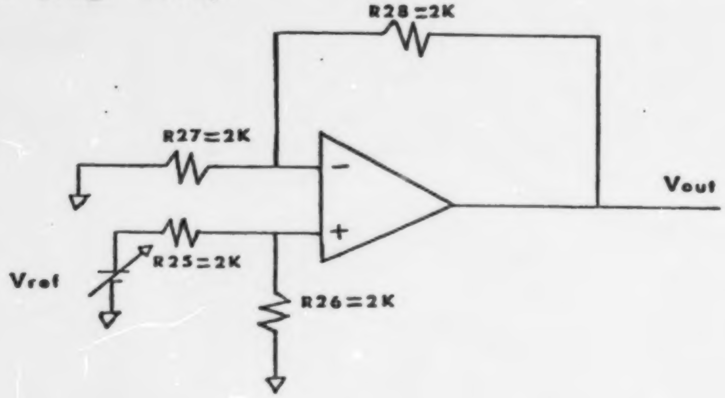


Figure 4.7d

At point b, we have $Vb = Vref \; \frac{R26}{(R25 + R26)}$

$$= Vref \; \frac{2.0K}{(2.0k + 2.0k)}$$

$$= \frac{Vref}{2}$$

The output voltage (Vout2) is

$$Vout2 = (1 + \frac{R28}{R27}) * Vb$$

$$= (1 + \frac{R28}{R27}) * \frac{R26}{(R25 + R26)} * Vref$$

$$= (1 + 1) * \frac{Vref}{2}$$

$$= Vref$$

Therefore, $V_{out} = V_{out1} + V_{out2}$

$$= -V_{in}\frac{R28}{R27} + \left(1 + \frac{R28}{R27}\right)\left(\frac{R26}{R25 + R26}\right) * V_{ref}$$

$$= V_{ref} - V_{in}$$

As we can see, by varying the reference voltage (Vref) we get a fine tuning adjustment to optimize the signal at the A/D converter. If fine tuning is not required, then this part will be taken out with an aid of a jumper from the subtractor to the A/D converter section.

The fine tuning should be set to exactly duplicate the desired input signal (reversed polarity) by removing unwanted offsets. The normal operating Radar signal at the output of this stage would be 0 to -2 volts.

4.2.9 Analog-to-Digital Converter (A/D).

The TDC1048 Analog-to-Digital Converter is used to convert the analog signal to 8-bit digital Radar words (DIG0-7), which is supplied to the FIFO section of the Digitizer Digital section.

The A/D converter consists of 255 clocked latching, comparator, combining logic, and output buffer register. The output latch holds the output digital Radar words constant between updates.

The TDC1048 operates from two power supply voltages, +5.0 V and -5.0 V.

The TDC1048 converts analog signals in the range VRB to VRT into digital form. VRB is the voltage applied to the pin at the bottom of the reference resistor chain and VRT is the voltage applied to the pin at the top of the resistor chain (see Figure 4.2.9.1). It should be between +0.1 V and -2.1 V. The voltage applied across the reference resistor chain should be between 1.8 V and 2.2 V. The nominal voltages for VRT = 0.0 V and for VRB = -2.0 V. A special circuit has been added between the op-amp stage and the A/D converter (fig. 4.10). It's function is to protect positive voltage to be applied at the Vin input pin of the A/D.

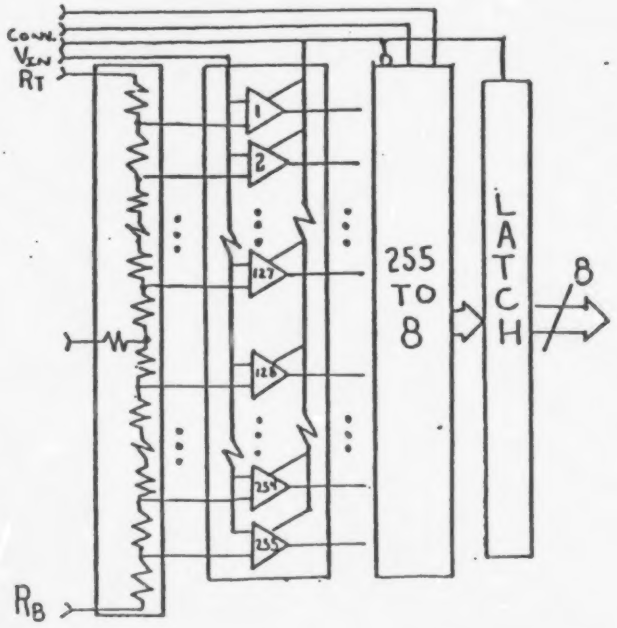


Figure 4.8. Functional Block Diagram of TDC1048

A midpoint tap, RM, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary. The characteristic impedance seen at this point is approximately 220 Ohms, This should be driven from a low load-impedance source. Note that any load applied to this point will affect the linearity of the A/D converter, and noise introduced at this node will degrade the performance of the quantization process. RM is an alternate input point for application of STC and gain.

The TDC1048 requires a convert (CONV) signal to operate. The Digital clock (DIGCLK) pulse is supplied by the Digitizer Digital section to this pin (CONV) for the operation. A sample is taken (the comparators are latched) within 15 nanosec after a rising edge on the Digital Clock pulse. The 255 to 8 encoding is performed on the falling edge of the DIGCLK signal. The coded result is transferred to the output latches on the next rising edge. The Digital Radar data is held valid at the output register for at least the output Hold Time, after the rising edge of DIGCLK. New data becomes valid after a Digital Output Delay time. This permits the previous conversion result to be acquired by the Converter Board at that rising edge i.e. Digital Radar data for sample N is acquired by the Converter Board while the TDC1048 is taken input sample N+2 (see Figure 4.9).

For optimum performance, the input impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1048 if it remains within the range of VEE to +0.5 V. Protection is supplied to limit the positive input voltage so that the TDC 1048 will not be damaged. If the input signal is between the VRT and VRB references, the output will be a binary number between 0 and 255 inclusively. A signal outside this range will indicate either full-scale positive or full-scale negative, dependent on whether the signal is off-scale in the positive or negative direction.

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum Holding time after the rising edge of the Digital Clock pulse. For optimum performance, 2.2 kOhms pull-up resistors are used.

Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These resistors are shown as R1 and R2 in the Functional Block Diagram of TDC1048 (Fig.4.8). Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above calibration method requires that both ends of the resistor chain, RT and RB, are driven by buffered operational amplifiers. Instead of adjusting VRT, RT can be connected to analog ground and the 0 Volt end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to RB. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

The bottom reference voltage, VRB, is supplied by an inverting amplifier, buffered with a PNP transistor (2N2906). The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The inverting operational amplifier provides a slight gain for fine calibration.

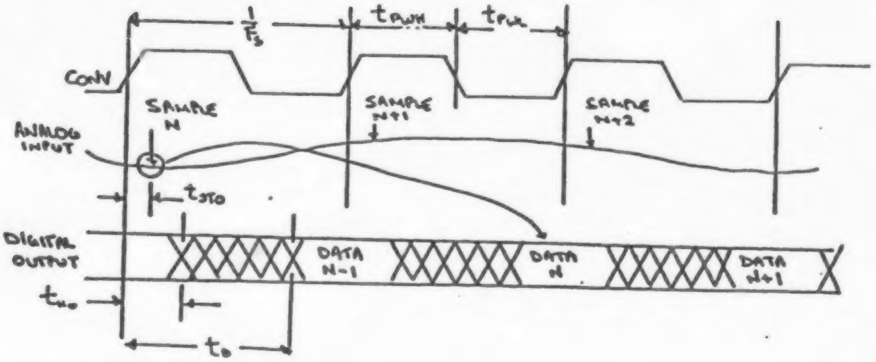

$\frac{1}{F_S}$
t_{PWH}
t_{PWL}
CONV
SAMPLE N
SAMPLE N+1
SAMPLE N+2
ANALOG INPUT
t_{STO}
DIGITAL OUTPUT
DATA N-1
DATA N
DATA N+1
t_{HO}
t_D

Figure 4.9. The Timing Diagram of TDC1048

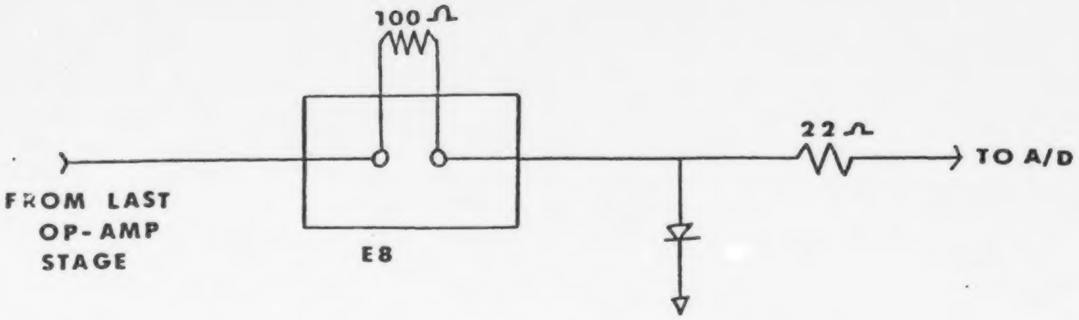

100 Ω
22 Ω
FROM LAST OP-AMP STAGE
E8
TO A/D

Figure 4.10 A/D positive voltage protector.

4.3 Digitizer Digital Section

The basic timing of the DIGITIZER board is a 40 MHz oscillator located at SPARE 3 (see ECOs). The output of the oscillator is fed directly to the count-up input of u23. All digitizing and STC timings are generated from this source. The oscillator may be decreased for different applications.

Two 4 bit binary counters (74F193), U23 & U18, are used to generate the frequencies needed for the sampling of the radar signal (DIGCLK) and the STC output to the DAC (STCCLK). Eight frequencies are available for both DIGCLK & STCCLK. Table 1 shows the bits to set on the converter to select which frequency for those signals. Selector/Multiplexer U19 & U24 choose 1 out of 8 inputs from the counters.

One-shot U10 is used for enabling and shaping of the RADAR TRIG input. The pulse created (NT) resets and starts the sampling of 256, 512, or 1024 Radar words to be written into the Digitizer RAM section. It uses a positive edge triggering operation. The triggers are fed thru only when the signal (TRIGSTOP) is inactive (low). In front of U10 is a voltage divider to accommodate for trigger voltage higher than 5 Volts. Table 2 shows the resistors needed for different input voltage. For more accurate coupling of the RADARTRIG signal, a formula is supplied to get exact resistors for different input impedance and voltage.

TRIGGER INPUT VOLTAGE	R33 ohms	R34 ohms
2.5V	SHORT	OPEN
5.0	SHORT	OPEN
7.5	390	560
10	560	510
15	680	330
20	750	220
25	820	200
30	820	150
35	820	120
40	910	120
50	910	100

One-shot U16 is a pulse-shaper for the CONVERT signal going to the A/D converter. Its job is to make a pulse the exact width at the exact time. Its output is derived from DIGCLK, it should be of the same frequency.

Counters U33, U34 and U35 are used as 4 bit up-counters to generate the 11 write addresses to the RAM. This address is incremented on each falling edge of DIGCLK. So, for each radar input sample, there is a new address to the RAM. This count is reset to zero for every trigger let thru by U10, making sure the address is 0 at the start of each radial.

Multiplexers (74F157) U38, U39 and U40 are used to select the proper address (RAMADD1-8) to be used in the read/write random access memory device (93422) of the RAM section. When a sampling time-slot is active, the multiplexers let thru the outputs of the counters, the rest of time being allocated for addresses coming from the converter. The write to the RAM from the sampling section is sequential, but the reading of the RAM by the converter is random. The outputs of the multiplexers give 10 bits of addressing (1KByte). The most significant bit selects which 256 bit bank to access, LOWER or UPPER. The least significant bit selects the EVEN or ODD bank. This scheme effectivelly doubles the throughput of the RAM.

The '157 is a quad 2-input multiplexer. It selects four bits of data from two sources (SCADD0-9 and WRA0-10) which are under the control of a common Select input (COUNTERSTOP). The Enable input is active LOW. When Enable is HIGH, all of the outputs are forced LOW regardless of all other inputs.

The three most significant bits of the counters (8,9,10) are anded with 3 bits from the converter (LENGTH0-2) to produce the COUNTERSTOP signal, which decides when sampling stops, after 256. 512 or 1024 samples. When COUNTERSTOP = 0, sampling is enabled.

Parallel Digital Radar Data (8 bit), from the analog section, is latched using D-Type Flip-Flops (74F374) U43 & U44. The clock signal to latch the data comes from DIGCLK anded with ODD or EVEN.

The RAMADD0 signal determines whether an Even or Odd RAM Section is to be used. This enables the proper buffer Clock (CP) of 74F374 U43 or U44 (ELTCH and OLTCH) to latch the new data and permits a write pulse (/WE) on the selected RAMs by deactivating the Clear input of 96LS02 U49 (EVEN or ODD side).

The Read and Write operations are controlled by the state of the active LOW Write Enable (/WE) of the 93422 Random Access Memory device. With Write Enable held LOW and the device selected, the data at Din is written into the address location specified by RAMADD1-8. To read the data from the RAM, Write Enable (/WE) is held HIGH while the device is selected.

The Write Enable is controlled by two one-shots (96LS02), U49, one half for the even and the other for odd bank of RAM. WPLS is used in the timing of the Digital Clock pulse in order to trigger the Write Enable (WE). The operation is from Low to HIGH Voltage Level transition. The ODD and EVEN pulse are used to reset (Clear) the one-shots. At all time, one of the pulse is in the reset mode, and the other in the trigger mode.

Triggering Truth Table

A	B	Clr	Operation
High	Low->High	High	Trigger
X	X	Low	Reset

X are don't care

If the AVERAGE bit is ON on the Converter Board, then the averaging circuit will process 4 radials before sending one to the converter. This processing consists of adding samples at the same range position on four successive radials and then scaling by four the total into 8 bit data. Binary adders U32, U37 and U42 are adding for the even side, and U41, U45 and U46 for the odd. The result is then written to Ram, 10 bit wide unscaled. When data is read out of the Ram, if averaging is ON, the data is scaled down 2 bits, else it goes unchanged. This is done with the help of U25 & U29 for the even section and U26 & U30 for the odd. The last multiplexers U20 & U21 select which RAM block will go to the converter, the even or odd.

The converter board makes signal /1STRAD go low on every radial when averaging is off, or low only on the first radial out of four when averaging is on. This signal, when low, puts to 0 all hex flip-flops U47, U48, U50 & U51, adding 0 to each sample. This inhibits the first radial, when average is on, to be added with old data in the latches, or to disable averaging (adding) when bit not set.

The AVERAGE bit should be on only when the PRF is sufficiently high, or the antenna RPM is sufficiently low, that four complete radar pulse times are available between each of the 1024 radials per revolution. The worst case (shortest) timing between radials is the value of importance. Effects of wind and gearbox freeplay on antenna speed can be quite large. AVERAGE should only be used with the MK-127 radar when short pulse is used.

$$PRF / [\ 1024 / (\ 60 / RPM\ )\ ] \geq 4$$

where RPM = max. momentary speed of antenna
NOT average rotation rate

5.1 SYNCHRO BOARD OVERVIEW

The SYNCHRO TO DIGITAL CONVERTER board is a stand alone circuit used to provide a digital antenna pointing word utilising the synchro, resolver or direct sine-cosine signals generally available from a radar system. The board is packaged as a narrow width, double height Eurocard circuit for placement in either the front or rear card cage of a standard Eurocard chassis. The main components of the circuit are;

a. SDC-632 type, industry standard synchro to digital converter.

b. RDC-19200 type resolver to digital converter.

c. Electronic Scott-T transformer

At any one time either the SDC-632 or the RDC-19200 component may be used, but not both. The 632 device is an industry standard package (second sourced) but is expensive and is also limited in the number of different signal formats which it will accept. On the other hand, the RDC-19200 is less expensive and can accept most any antenna position signal and voltage with two versions. The digital data is available at a 26-pin ribbon cable header which is connected to the CONVERTER board. The 632 can supply up to 14 bits of information while the 19200 can supply 16 bits.

5.2 SYNCHRO OPERATION

5.2.1 SDC-632 TYPE

Only the input synchro scaling resistors R11 through R13 may be utilised if the synchro voltages are non-standard. Otherwise, place the proper version of the 632 on the board and short R11 - 13. The Scott-T is not used. There is also a scaling resistor R16 in the Reference line which should be set or shorted accordingly.

5.2.2 RDC-19200 TYPE

The RDC-19204-302 (11.8 V) or RDC-19206-302 (90 V) synchro components should be used. The input scaling resistors must be set according to the input synchro voltages. The Reference (RH) scaling resistor must also be set to prevent damage to the device. The RDC-19200 will accept most synchro signals of sinusoidal, square or triangular format. The device is specified for 400 Hz and higher Reference frequencies, but will operate properly at 60 Hz Reference for typical slow turning navigation radars.

5.3 RESOLVER OPERATION

5.3.1 SDC-632 TYPE

Only the input resolver scaling resistors R11 through R14 may be utilised if the resolver voltages are non-standard. Otherwise, place the proper version of the 632 on the board and short R11 - 14. The Scott-T is not used. There is also a scaling resistor R16 in the Reference line which should be set or shorted accordingly.

5.3.2 RDC-19200 TYPE

The RDC-19200-302 or RDC-19201-302 components should be used. The Scott-T is not required for resolver operation in conjunction with the resolver version of the 19200. The input scaling resistors must be set according to the input resolver voltages. The Reference (RH) scaling resistor must also be set to prevent damage to the device. The RDC-19200 will accept most resolver signals of sinusoidal, square or triangular format. The device is specified for 400 Hz and higher Reference frequencies, but will operate properly at 60 Hz Reference for typical slow turning navigation radars.

5.4 DIRECT INPUT OPERATION

5.4.2 SDC-632 TYPE

There is no 632 version for direct sine, cosine input.

5.4.2 RDC-19200 TYPE

The RDC-19202-302 or RDC-19203-302 components should be used. The Scott-T is not required for direct input operation in conjunction with the direct input (2 volt) version of the 19200. The input scaling resistors must be set according to the input voltages. The Reference (RH) scaling resistor must also be set to prevent damage to the device.

5.5 JUMPER SETTINGS

JUMPER #	SYNCHRO 1920X	SYNCHRO 632	RESOLVER	DIRECT	FNCTN
E1	OUT	OUT	OUT	IN	VEL. *
2	1-4	1-4	1-4	1-4	RL
3	IN	IN	IN	IN	S1, R1
4	OUT	OUT	OUT	IN	V *
5	OUT	OUT	OUT	OUT	COS *
6	IN	IN	IN	IN	S3, R3
7	OUT	OUT	OUT	OUT	SIN *
8	IN	IN	IN	IN	S2, R2
9	IN	OUT	IN	IN	BW *
10	OUT	OUT	OUT	OUT	A *
11	IN	OUT	IN	IN	B *
SCOTT-T	OUT	OUT	OUT	OUT	SCOTT-T **

* - USED ONLY WITH 19200

** - SCOTT-T COMPONENTS, 1458 OP AMP (U1) AND ASSOC. RESISTORS R1 - 10.

6.1 DIRECTIONS ON USE OF RADAR COMPONENTS

This section is included as an application guide for the various programmable features of the radar scan converter equipment. It should be noted that no two radar sets are the same, as far as their radar video signals are concerned, so the user should design the appropriate flexibility into the application software. Radar signal processing and display are not simplistic tasks. Successful completion of projects such as target detection and tracking relies strongly on the acquisition of knowledge and experience in the radar field. Many of the features to be discussed were implemented due either to experience or to afford maximum flexibility to the subsystem. As a result, it should be possible to design many software systems around the scan converter. If a particular software application cannot be implemented with the current radar hardware, consult INTEGRAD for information on the modification of the scan converter to meet your requirement.

6.2 STC OPERATION

The programmable STC (gain, attenuation) capability of the radar subsystem is designed to allow the application software to apply a range (time) based gain to the input radar video in order that the digitised samples can be normalised in amplitude over a specified range interval. This is necessary because of the widely varying power returns from irradiated targets at different ranges (distances) from the radar antenna. The programmable STC (hereinafter called PSTC) affords more control and precision as well as repeatability compared to the conventional STC supplied with the radar equipment. The conventional STC is essentially an RC network which approximates the power decrease function of a real marine radar. The PSTC can be programmed to reflect the real radiation geometry under virtually all sea conditions. The PSTC can also include D.C. components to move the normalised video up and down through bit windows to capture intensities of interest. Note that the PSTC is most effective when coupled to radar systems which incorporate a log amplifier. Linear amplifiers saturate to detect and therefore do not present range dependent amplitudes. Note also that the DIGITIZER, as supplied, does not normalise the radar video to the full input range of the A/D converter. There are several optional methods of applying the PSTC and fixed gains of the DIGITIZER board which require changing component values and/or jumper wires only. These will be discussed later.

6.2.1 MARINE RADAR RADIATION

The radiation pattern of a marine radar is described by its main horizontal and vertical beamwidths and by its secondary side beamwidths. A parabolic antenna would have equal horizontal and vertical beamwidths while a typical marine slotted-waveguide (stick) antenna would have a vertical beam of 25 degrees and a horiz. beam of 1 deg. The specified main beamwidths are those angles centered about the axis of the antenna at whose extremities the received power is one-half (-3dB) that received along the axis. The secondary power points are defined either as power readings at a set angular separation (say 10 deg. off the main beam) or as angle measurements for the important power levels (-20 and -30 dB). These values change from one radar to the next.

Eqn. 6.1 $\quad$ dB = 10 log [P1/P2]

-3dB implies P1 = 2*P2
-30dB " P1 = 1000*P2

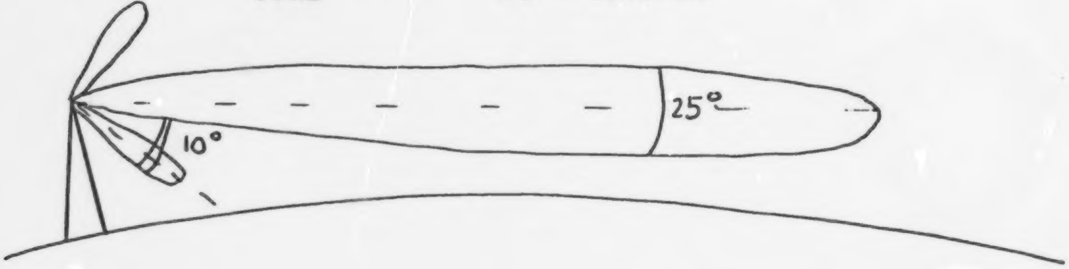


figure 6.1 TYPICAL VERTICAL BEAM PATTERN

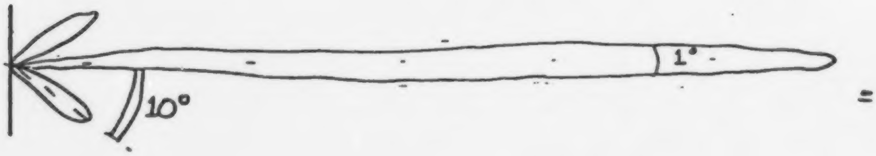


figure 6.2 TYPICAL HORIZONTAL BEAM PATTERN

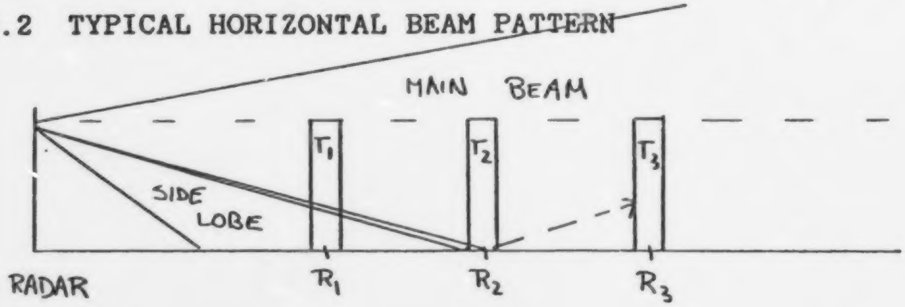


figure 6.3 VERTICAL RADAR GEOMETRY

In figure 6.3, the power received, per unit area, at each range Rn from the radar falls off roughly as the square of the distance (1/Rn**2). Complications here include reflections from the sea surface. Reflected energy from the targets also decreases as the square of the distance from the antenna. For a point target (long range), the radar will thus receive power relative to the fourth power of the range (1/R**4) to the target. For a target such as T2, where all the main vertical beam power is reflected, the power loss would be restricted to the square of the range along the return trip to the antenna. If T2 had only half the height shown, it would receive only half the original power and subsequently the radar would detect less energy. Similarly, if the target was T3 at a longer range where it received half the power, but with the same height, T3 would reflect this half power and the radar would receive an even lower level because of the extra (1/R**2) range loss. Any targets (T1) inside the area covered by the secondary beam (side lobe) would reflect a greater amount of radar energy. This area also gives rise to the worst sea clutter returns. The radar antenna height factors heavily in defining this region.

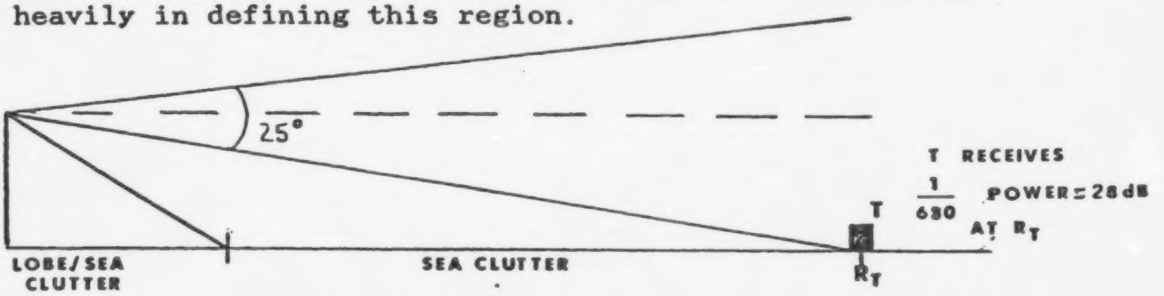


figure 6.4 SEA CLUTTER GEOMETRY

The STC equation (6.2) which defines the attenuation to be applied to the radar-received power from targets which receive the full beam is;

Eqn. 6.2 dB(r) = -6 [(log r - log R) / .3] for 1/r**2

where r = target range
R = max. range which fills beam

For targets past this range;

Eqn. 6.3 dB(r) = -12 [(log r - log R)/.3] for 1/r**4

where R = max. detectable range

To complicate matters, the complete STC equation must take into effect both the horizontal and vertical forms of these equations. That is, different R's for horiz. and vertical.

For each interval over which an STC equation is applied, divide the power attenuation (dB(r)) by the dynamic range (in dB's) of the interval and then multiply by the digital scale to get the digital attenuation for each range element;

Eqn. 6.4 $PSTC(r) = dB(r)/dBtotal * (Dstc)$

where Dstc max. = 256 because the
DIGITIZER D/A is an 8-bit device

In practice, the PSTC should be chosen less than 256. The Dstc max. should be chosen to provide an A/D output digital value at close range equal to that output from the target at the desired normalised range R. For simplicity, the equation 6.2 can be used employing R as the distance at which the horizontal beam becomes larger than the targets of interest. For a target of horizontal extent of say, 50 meters, the range R would be;

Eqn.6.5 $d/R = 50/R = \sin(1 \text{ deg.})$

$R = 2860$ meters

$\log R = 3.456$

Putting these values into equation 6.2 ;

Eqn. 6.6 $dB(r) = -6 [(\log r - 3.456)/.3]$

r in meters

$PSTC(r) = dB(r)/dBtotal * Dstc$

$dBtotal = dB(r \min)$

if r min = 10m, dBtotal = 49.12

The value 6 in equation 6.6, which represents one quarter the power (10log1/4) for each halving of the range, can be varied to simulate the decay rate of the conventional STC. Similarly, the value R can be varied to simulate the STC initial charge. Additional d.c. levels can be added to the PSTC to normalize further over areas of side lobe importance and to account for extra power received from the sea surface itself.

The range increments r in PSTC(r) are dependent on the setting of the STCSPEED register on the CONVERTER board. If STCSPEED = 0, then;

Eqn. 6.7 $r = 1/2 * c/f = .5 * (3*10exp8/20*10exp6) = 7.5m$

If STCSPEED = 4;

Eqn. 6.8 $r = .5 * c/1.25*10exp6 = 120$ meters

The PSTC can be set for a particular maximum range with the appropriate STCSPEED and the DIGSPEED can be varied as required. This type of operation obviates the need to continually change the PSTC. Alternatively, the PSTC can be reloaded for each different setting of DIGSPEED, in which case STCSPEED would have to be set accordingly. STCSPEED should be greater than or equal to DIGSPEED.

PSTC can be determined experimentally, for different size targets, by monitoring the RAB data values, with no STC, at different ranges from the radar.

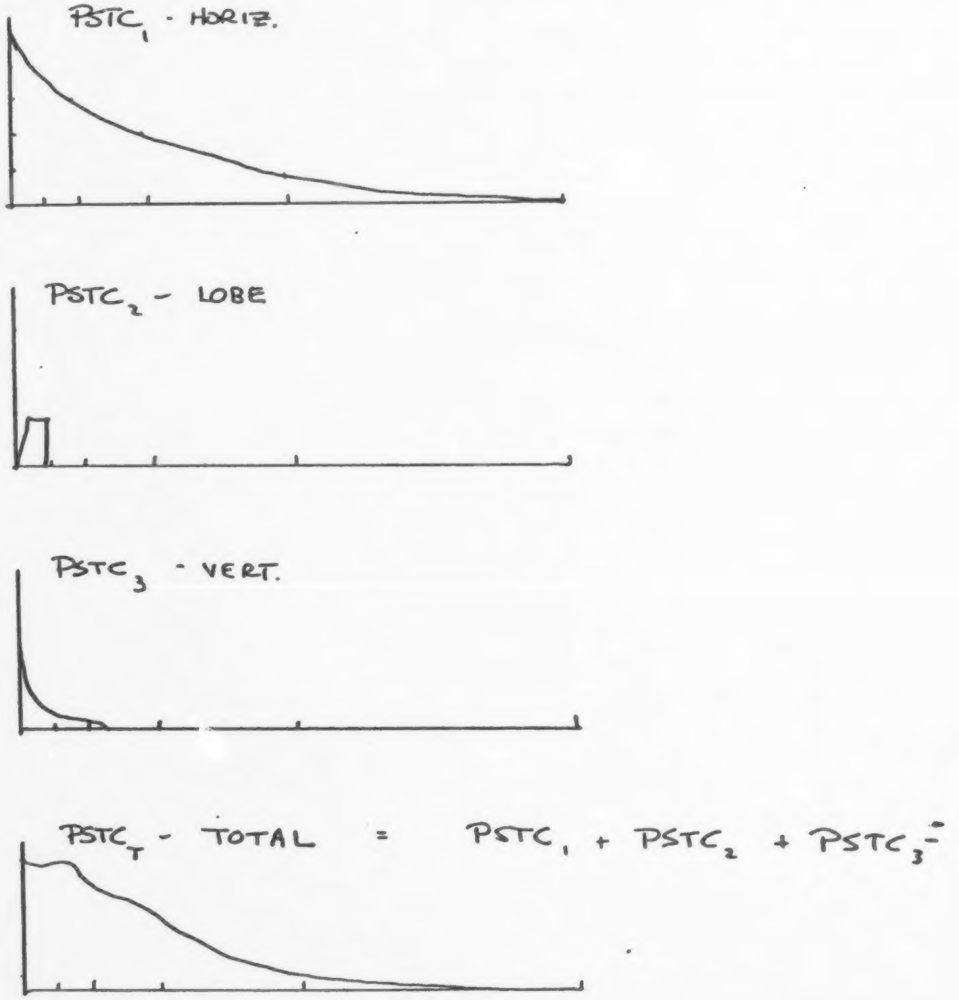


figure 6.5 EXAMPLES OF PROGRAMMABLE STC WAVEFORMS

6.3 OPTIONAL CIRCUIT OPERATION

Because the PSTC attenuates the radar signal, the resultant input to the A/D converter may not fill the 2 volt range of that device. It is possible, after having some experience with the radar subsystem, to change the fixed gain at the op-amp (U6) input to the A/D. Installing a fixed and/or variable resistor at R28 will allow the op-amp to run the A/D at full scale for the general case. Alternately, the PSTC voltage from U5 may be disconnected from U4 and tied to the A/D's reference input at jumper E7. The jumper should be removed in this case. This circuit will dynamically vary the gain of the A/D at the STCSPEED rate. The A/D may exhibit non linearities in this mode. No attenuation would be possible here, only positive gain. These circuit alterations should only be attempted by someone with analog and digital circuitry experience. Some voltage levels need to be verified to avoid damage to the components.

6.4 DIGITAL GAIN

Because the RIB function of the BUFFER board stores only a selected 2 bits of the RAB 8-bit data, the 4-bit gain function T0-3 was implemented to allow the programmer to add a value of 1-15 to the data. The T0-3 function is only active when the ADAPTIVE THRESHOLD or FTC are being used. These functions can cause a great decrease in the resultant RAB data values as they are high frequency filters and edge detectors. The application of T0-3 can help to move the data values up so that they can be contained in a 2-bit RIB window. In this way, desired target intensities may be read in one pass of the RIB and the diagnostic display will present all important targets. If, in a particular case, all the ADAPT and FTC data are high in intensity (linear amplifier), the T0-3 function will have little or no effect. However, in the case of widespread rain or sea clutter, the T0-3 function can be used to position the sea and weather clutter just below a 2-bit RIB window allowing the stronger target returns to reside in the next RIB window. See figure 6.6.

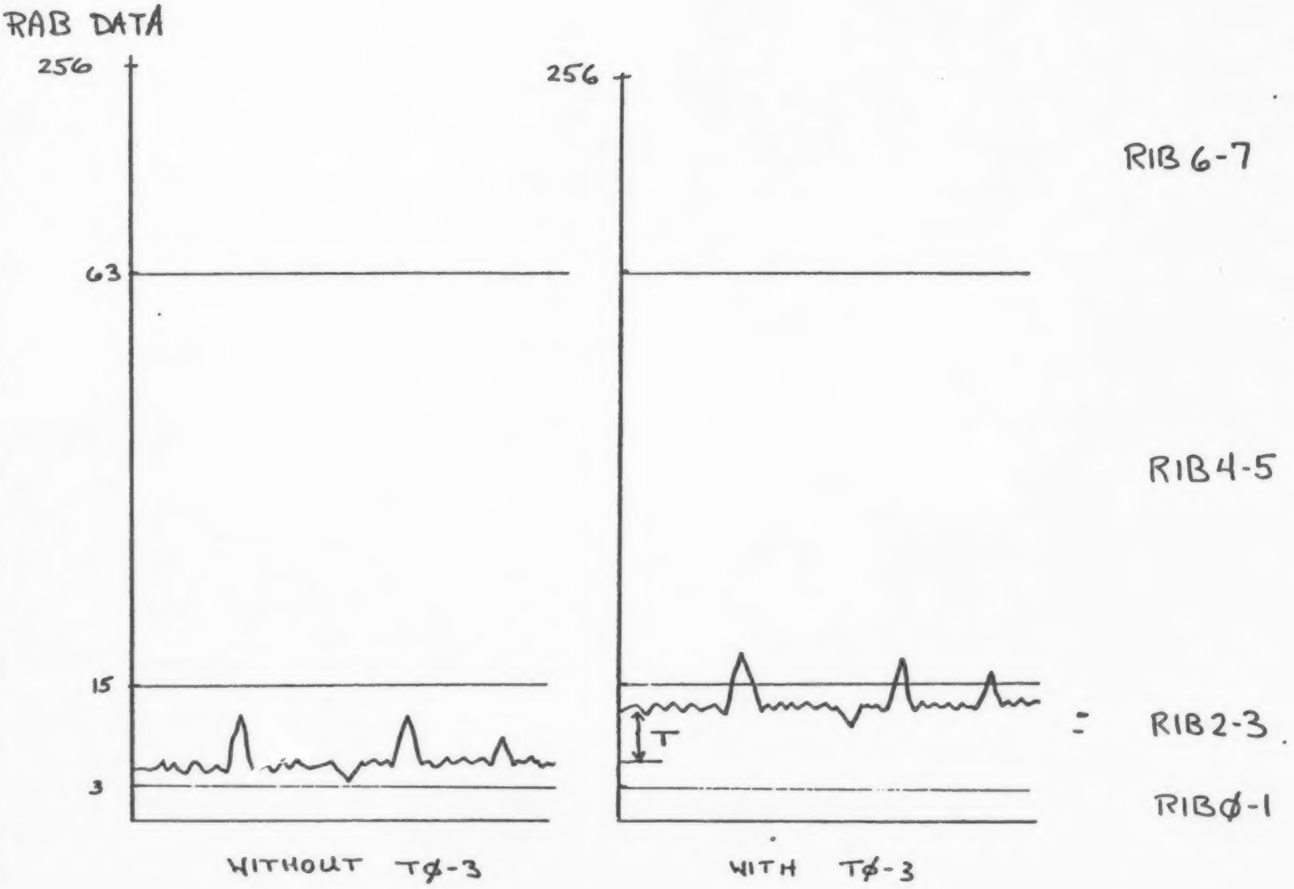


figure 6.6 EXAMPLE OF T0-3 FUNCTION

compass stabilized'; it is a *relative* presentation, i.e. movements of other ship's echoes on the screen are relative to that of own ship.

In one radar design, it is possible in the *true motion* presentation to turn the picture so that it is stabilized with ship's intended course upwards, instead of with north upwards. The heading flash will point to 0° when the ship is heading the intended course, and will move if the ship deviates from this course. This presentation is called 'true motion with ship's intended course upwards'.

The three positions of switch 1 in *Figure 9.31* are then as follows:
(*a*) Ship's head upwards, unstabilized.
(*b*) North upwards *or* ship's intended course upwards, compass stabilized.
(*c*) Track indication (i.e. true motion), with north upwards *or* ship's intended course upwards, compass stabilized.

In positions (*b*) and (*c*), the picture may be turned, by means of the alignment control, to the 'north upwards' or 'ship's intended course upwards' position, or if necessary to any other position.

RADAR SPECIFICATIONS

The performance of a radar depends on various interrelated specifications, which will now be discussed.

Pulse duration and pulse-recurrence frequency

In a previous example, it was assumed that a pulse with a duration of 0.1 μs was produced 1000 times per second (the p.r.f.). Therefore between the beginning and end of this pulse lies a time span of 1/10 000 000 s. As the velocity of propagation is about 300 metres per microsecond, the start of the pulse will be about 0.1 × 300 = 30 m from the scanner at the very moment the end of the pulse is leaving the scanner. So when the pulse duration is 0.1 μs, a pulse about 30 m long is sent into space.

Range discrimination

Now suppose that this pulse meets an object of very small dimensions on its way. The echo is, of course, as long as the outgoing pulse (i.e. 30 m) and thus the length of the echo on the screen in a radial direction corresponds to 30 m. Note that the distance at which the object is located is immaterial.

Now assume that this pulse meets two objects on its way, P and Q, located in the same direction, one 15 m behind the other (the object P is so small that it causes no appreciable shadow in the outgoing radiation); this is depicted in *Figure 9.32*. It will be clear that the beginning of Q's echo reaches P just as the end of the outgoing pulse is passing P. The echo pulses originating from P and Q are therefore contiguous, and the objects P and Q will not be made visible on the screen as two distinct echoes but as one 'merged' echo. If P and Q are more than 15 m apart, a separate echo will be seen from each. The size of the spot of light on the screen, which might affect unfavourably the observation of the two distinct echoes, is ignored here.

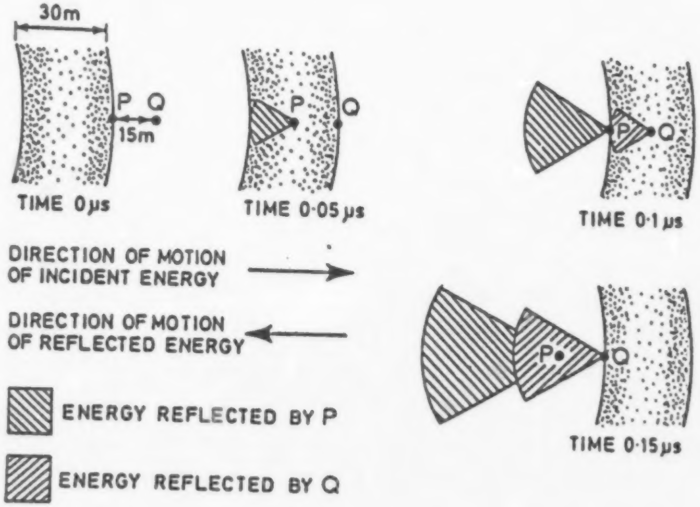


Figure 9.32 Pulse duration and range discrimination. Two targets, P and Q, are on the same bearing but differ in range by 15 m; the four diagrams show the progress of the incident and reflected energy of a 0.1 μs pulse (length 30 m) passing these two targets

The minimum distance in radial direction at which two objects will be reproduced separately is called the 'range resolution' or 'range discrimination'. It is equal to half the pulse length and is thus proportional to the pulse duration.

To be able to observe separate echoes from objects a short distance apart, the pulse should be short. It is now technically possible to generate reliable high-powered pulses of 0.05 μs and less. This corresponds to a theoretical range discrimination of 7.5 m or less. Most makes have a shorter pulse duration on the smaller ranges than on the longer ones (see under 'Pulse duration').

In practice the range discrimination of the various makes lies between 10 and 30 metres.

Pulse duration

On longer ranges, the discrimination is equal to more than half the length of the pulse, and is therefore less favourable. It is affected then by the size of the light spot on the screen.

The smallest possible diameter of the light spot is about 0.25 to 0.125 mm. If the radius of the spot is, say, 0.125 mm, the smallest distance on the screen between two echoes that can just be distinguished apart is 0.25 mm. With a 12 in (≈ 300 mm) screen this corresponds to a distance of about 125 m on the longest (40 miles) range. On longer ranges there would therefore be little point in using a short pulse duration. A longer pulse means, moreover, increased energy of the outgoing pulse and of the echo, so that 'targets' hit by the beam will be better detected. In order to protect the magnetron against overloading due to a long pulse, the number of pulses per second is sometimes reduced automatically. On longer ranges the pulse duration is therefore in most sets longer and the pulse-recurrence frequency (p.r.f.) lower than on a smaller range.

There is one radar design in which it is possible by means of a special switch to choose between a pulse duration of 0.1 μs (p.r.f. 1000) and 1.0 μs (p.r.f. 500). This choice can be made only on the intermediate ranges.

When the aim is to make visible objects *at a large or a small distance*, a long pulse duration should be chosen so that the energy of the echo is increased. In the case of a short pulse duration, however, the lengths of the pulses in space (and thus the lengths of the echoes) decrease and a more detailed picture is obtained. This applies as well to faraway as to nearby objects. For detecting a buoy in sea-echoes, for instance, a short pulse duration is preferable.

Minimum range

It is evident that the pulse length also determines what is called the 'minimum range' of a radar set. It would not be possible to receive the complete echo of an object if the start of its echo had already returned before the end of the pulse train had left the scanner. For a pulse length of 0.2 μs, this minimum range is theoretically 30 m, but in practice it is longer. Moreover, the receiver is not able to detect an echo immediately after the very powerful transmitted pulse has left the scanner. The minimum range is consequently a little longer than half the length of the electromagnetic pulse; it may be assumed to be 15 to 30 m, depending on the pulse length and other factors. A short pulse duration is thus favourable to both range discrimination and minimum range. Technical development will probably shorten pulse durations still more in the future, but so long as pulses are used the minimum range will not be reduced to zero.

Range accuracy

The accuracy to which the distance from an object may be determined with the variable range marker is about 1½ per cent or better of the radius of the range to which the radar is switched. On the 12-mile range the error of any distance measured may consequently amount to 0.015 × 12 = 0.18 n. mile.

The range accuracy depends largely on the correct adjustment (see page 268) of the variable range marker with respect to the fixed range rings. The fixed range rings are more accurate than the variable one; their accuracy should be determined (for example when the ship is in port) by comparing the range of a radar-conspicuous point on the chart with the range as displayed on the radar screen.

Power

The power of radio-frequency oscillations generated in the magnetron during the transmission of the pulse is called maximum or peak power. If the same quantity of energy were generated continuously rather than in pulses, the power, of course, would be much less.

Horizontal and vertical beam width

A car's main headlights send out light in the form of a beam. Some of the light is also, however, radiated to the sides, as is readily noticed when standing alongside the car. It therefore becomes difficult to determine the width of the beam of light in terms of degrees. The same difficulty arises with the radar beam radiated by the directional aerial. *Figure 9.33* shows the field strength in azimuthal directions. In practice, it is agreed to take as the beam width the angle between the lines OB and OC, which are located so that the power output in these directions is half the maximum OA. Points B and C are called the 'half-power points'. (Instead of the angle between the half-power points a larger angle is sometimes given.)

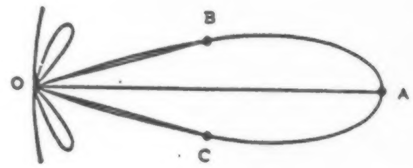


Figure 9.33 Power in azimuthal direction. OB = OC = ½OA, B and C are half-power points; angle BOC is horizontal beam width, which is exaggerated here (it is usually only 0.6–2.0°)

The horizontal beam width of ship radar installations usually lies between 0.6° and 2°. When we look at *Figure 9.33* we should bear in mind that the beam width is much smaller than it is represented there.

If a small beam width is desired, the wavelength used must be small compared with the span of the reflector. This is of importance in the design of the installation. It is impossible to increase the dimensions of the reflector without limit, for this would cause difficulties of a mechanical nature.

In nearly all cases the transmitting aerial also serves for receiving. Now it can be shown that a diagram that shows the radiated power when the aerial is used for transmission also indicates the power received from various directions when it is used as a receiving aerial. It is evident that the directional effect of an aerial used for both transmitting and receiving is thus increased still more.

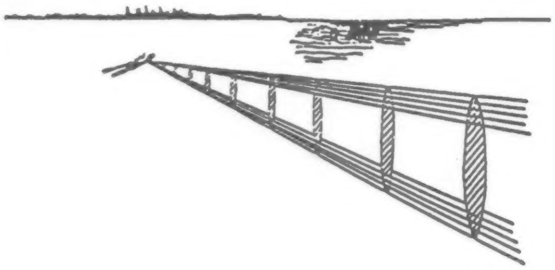


Figure 9.34 Ship with radar beam

The beam width in the vertical plane is made considerably larger. This is done to prevent echoes from being missed because of the ship's rolling and pitching. The angle for this vertical beam width is 15° to 30° (see *Figure 9.34*). Any desired beam width may be obtained by changing the shape and proportions of the scanner, just as any desired beam of light may be obtained by using appropriate reflectors. Radio waves are of similar nature to light waves and their reflection obeys the same laws. They differ only in wavelength.

Side lobes

Figure 9.33 shows the power in various directions in the horizontal plane and demonstrates that, in addition to the main beam, some energy is also transmitted in other directions. To eliminate these *side lobes* altogether, the reflector would need to be very large. In practice, a compromise is sought, and side lobes are tolerated to some extent. Instead of the two side lobes shown in *Figure 9.33*, there are usually a great many.

Obstacles located in the path of side lobes are also struck by the radar pulses, though these pulses have less energy, For clarity, the side lobes in *Figure 9.33* are shown too large compared with the main beam. The power in all side lobes together is usually about ¼ per cent of that in the main beam.

Later it will be shown that side lobes give rise to false echoes.

Lobes in the vertical plane

A closer examination of the radiated pattern in the vertical plane shows that it consists of a great number of lobes of the shape shown in *Figure 9.35*. The cause is the surface of the sea, which reflects the radiation.

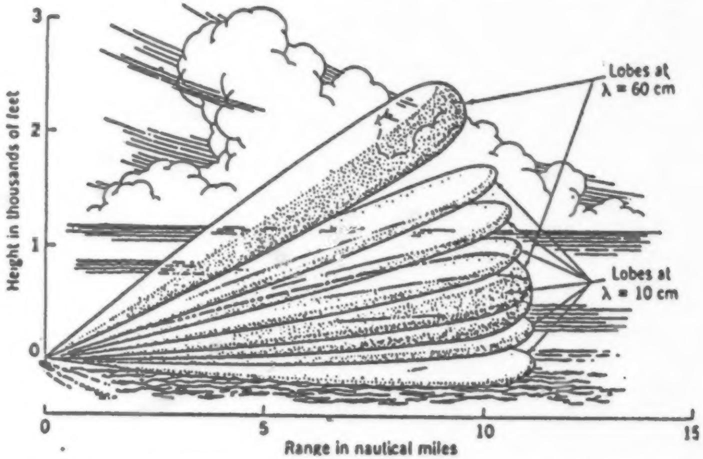


Figure 9.35 Lobe structure for 10 cm and 60 cm radiation over a flat reflecting surface (from Radar Aids to Navigation, *John S. Hall, courtesy McGraw Hill)*

Consequently the direct radiation ARP and the indirect radiation ABP will meet at a point P where they will wholly or partly reinforce or oppose each other (*Figure 9.36*). This depends on the difference in the path lengths ABP and ARP. What happens is comparable to fading due to the ionosphere, but note that a phase change of 180° takes place by reflection at B. If the difference in length between the paths at P were half a wavelength, corresponding to a phase change of 180°, then the total phase difference would be 180° – 180° = 0°. The two fields would thus be in phase at P.

Suppose that P' is located so that the difference in path lengths is one wavelength, then the phase difference will be 360° − 180° = 180°. Here the two oscillations neutralize each other, at least if we take it for granted that after reflection at B' no loss is suffered so that the two fields at P' are equally strong.

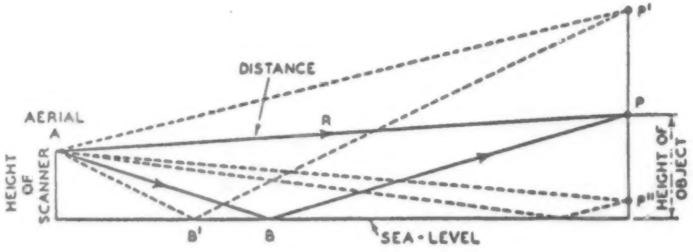


Figure 9.36 Direct and indirect radiation

For points immediately above the level of the sea, e.g. P'', the difference in path lengths is practically zero. Because of the phase reversal of about 180° on reflection, the two beams will neutralize each other at this point (even though they have travelled almost the same distance). *This is not favourable for the reproduction of very low objects.*

The number of lobes is in reality much greater than is shown in *Figure 9.35* and may amount to 500 for a wavelength of 3 cm.

When the sea is less calm (many sea-echoes) the reflection by the surface of the water is very diffuse and hence the minima between the lobes are, as it were, filled up.

To the navigation officer who, as a rule, is interested only in objects of small height such as ships, etc., the lowest of these lobes is the most important.

The lobes do not turn along with the ship when she is rolling or pitching. The difference in length between the paths at, say, point P in *Figure 9.36* is practically the same for a ship that is rolling and pitching as for one that is not.

Bearing discrimination

In *Figure 9.37(a)*, the horizontal beam width is such that the two equidistant ships A and B will be simultaneously struck by pulses, so that their echoes coincide. For the echoes to show separately the beam must be able to pass between the ships C and D without causing echoes (*Figure 9.37(b)*). The angle α between the ships must therefore have a minimum value somewhat larger than the horizontal beam width. This angle α is called the 'bearing discrimination' or 'bearing resolution', and is an important factor in a radar installation. It is clear that the angle in question does not depend on the distance at which the objects are located but chiefly on the beam width in the horizontal plane. In modern marine installations the bearing discrimination is from 0.6° to 2°. Even in the best types of ship's radar, this discriminating ability is about 30 times worse than that of the unaided eye and about 300 times worse than can normally be achieved with the aid of optical instruments.

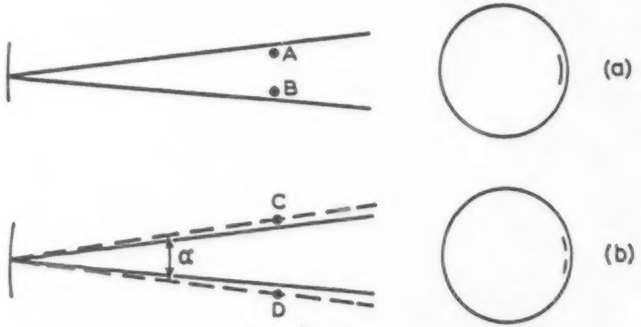


Figure 9.37 Bearing discrimination. (a) Objects A and B are too close for the beam to pass between them, so they merge on the screen. (b) The angle between A and B is wide enough for the beam to pass between them without causing echoes, so two separate echoes appear on the screen

Distortion in azimuth

Suppose that an object such as a factory chimney is struck by pulses and that the horizontal beam width is 2° (see *Figure 9.38(a)*). When the reflector is in the position OA the chimney is already being hit, so an echo is perceptible on the screen in the direction OA. Succeeding pulses hit the object, and this is only discontinued beyond the position OB of the reflector. Hence the point-like object is made to appear on the screen as an arc subtending an angle equal to the beam width. If we want the arc to be small, i.e. reduce the distortion, a small beam width is necessary.

Now take the case shown in *Figure 9.38(b)*. The object in fact subtends an angle of 10°, but on the screen its echo subtends an angle of 12° because the outer extremities of the object are already hit in positions OC and OD of the aerial. By reducing the gain, however, the object will be struck by little energy in the reflector positions OC and OD and the weak echoes will not be sufficiently amplified to be made visible on the screen; the echo-arc on the screen will thus become somewhat smaller.

There is another factor that influences enlargement of the subtended angle. An object with good reflecting characteristics such as a large ship needs to be struck by only a little radiation to reflect. A wooden mast, on the other hand, will give rise to an echo only when hit by powerful radar pulses. As a result the subtended angle is enlarged more for amply reflecting objects than it is for poorly reflecting ones.

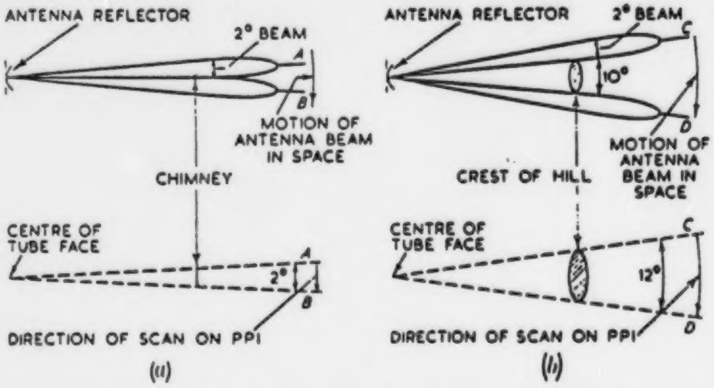


Figure 9.38 Distortion in azimuth: horizontal width of radar beam causes enlargement of echoes of (a) a chimney and (b) a long object

Since an echo's enlargement is expressed in degrees, its tangential dimensions will be greater the further it is from the centre of the picture. This can be observed on every radar picture. Consequently echoes from distant ships always give the impression that the ships are broadside-on (see, for instance, *Figures 9.21(b)* and *9.22(b)*). *Figure 9.39* shows variations in azimuthal distortion for ships at different ranges.

A small horizontal beam width offers the following advantages:

1. The bearing discrimination is improved.
2. The distortion in azimuth is lessened.
3. The energy will disperse less and remain more concentrated.

In order to obtain a sharp picture free of blurring and with all details clearly visible, the pulse length should be short and the horizontal beam width narrow. Pulse length and beam width therefore affect not only the two echoes behind each other (*Figure 9.32*) or side by side (*Figure 9.37*), however important this may be in some cases from a navigational point of view, but also the quality of the entire picture.

Bearing accuracy

A difference in alignment can arise between the motor shaft that drives the deflecting coils and the generator shaft driven by the scanner. It is clear that this can cause a bearing error which is slight in the case of accurate adjustment.

Bearing errors may also arise from the ship's rolling and pitching and the consequent movement of the beam. These errors are, however, so small that they need not be taken into account.

Thus the bearing accuracy of an accurately adjusted marine radar lies between 1° and 2°. In general terms, radar enables us to measure the distance to an object with reasonable accuracy, but a radar bearing is less accurate than a visual one. This is of importance in connection with radar position-finding.

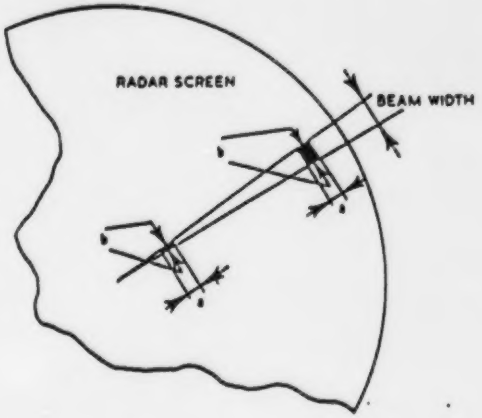


Figure 9.39 Variations in azimuthal distortion of echoes at different ranges: depths a are equal, widths b are not

Blind sector caused by the funnel

If the scanner does not protrude above the funnel, a blind sector must be taken into account. This is caused by the funnel intercepting the outgoing pulse and the echo, thus causing a radar 'shadow'. On some ships, this shadow can be observed on the screen, for instance when it cuts through a coastline. However, as the scanner is always mounted in front of the funnel, this blind sector will only impede 'radar view' behind, where it is usually not considered vitally important. The blind sector caused by the funnel may amount to an arc of from 10° to 45°.

Some shadow effect may also appear because of the foremast with its cross-tree and standing rigging. As energy is radiated over the entire width of the scanner, this shadowing is less than might be supposed, and is ordinarily present only on the short range scales. Nevertheless the intensities of the echoes of objects located dead ahead can be lessened by the effect of the foremast, as both the transmitted and reflected energy are weakened. This echo attenuation is such that it can reduce the maximum distance at which objects can be detected by a half or one-third. On normal cargo and passenger ships, with the usual distance between radar aerial and foremast, the sector of this weakening is small, from about 1° to 6°. This does not mean, however, that this blind sector can simply be ignored.

By mounting the scanner in front of the foremast or between the masts on the cross-tree of a twin-mast, shadows ahead can be eliminated.

When the ship is in port it is impossible even for experts to determine with certainty the precise effect and size of the blind sector or the sector of diminished view. It is therefore highly recommended that the master checks this at sea.

This can be done by observing to what extent the echo of a poorly reflecting object, for instance a small buoy, is affected when it goes into the blind sector of the display. Sea-return can also be used. A strongly reflecting object, for instance a coastline, is not suitable because its echo-energy, even when in the blind sector, is usually still sufficient after amplification to be reproduced on the screen.

If there is shadow-effect in the direction ahead, it is possible when navigating in fog to obliterate the blind sector by making small changes in course to port and starboard. The extent of the change in course depends on the size of the blind sector.

Maximum range

It often happens with a high sea that when echoes of distant ships are observed an echo will not appear on the screen with every revolution of the scanner, but can be missing for one or more revolutions. Because of the ship's pitching and rolling and the mass of water between the two ships, the pulses may not (or not adequately) strike the other ship for several scanner revolutions. The same holds true, at a smaller distance, for buoys. This is no indication that the installation is operating unsatisfactorily. This phenomenon is also caused by the fact that the reflecting power of some objects is subject to directional effects. Take, for example, a metal plate. Clearly this will reflect to a maximum extent if the radiation by which it is struck is directed perpendicular to the plane of the plate; the reflection will be reduced to almost nothing if the plane is parallel to the direction of the radiation.

The same effect can occur with ships, and even more often with buoys. Depending on the angle of incidence, the reflecting power will be greater or smaller; in the lapse of time between two consecutive 'irradiations' (2 to 10 seconds), differences may have occurred in the angle of incidence and reflection.

Later it will be seen that the distance at which an object is first observed is, in some measure, a means of ascertaining what kind of object it is; for instance, a buoy or a ship. This distance is usually taken as that at which the echo appears on the screen for 5 out of 10 scanner revolutions.

Number of scanner revolutions per minute

In every revolution, radar pulses from the rotating scanner must strike the object not once but repeatedly during the time it is aimed at the target. The effect on the screen of the repeated strikes will be cumulative, i.e. every echo-pulse received enhances the light-spot on the screen. Should insufficient pulses hit the target only a weak light-spot will be produced and this will disappear too quickly. The required number of pulses depends largely on the afterglow of the c.r.t. screen material.

The number of revolutions per minute of the scanner is between 20 and 30.

Wavelengths used in radar

If the transmitted electromagnetic energy is to be sufficiently concentrated in a beam without employing large reflectors, it is necessary (as already stated) to use very short wavelengths. Most marine radars make use of the X-band (wavelengths of 2.7–5.8 cm, i.e. about 3 cm).

The S-band (about 10 cm) is less frequently used. With this wavelength it is more difficult to obtain a narrow beam, as a result of which the picture is usually less detailed. On the other hand, radiation on a 10 cm wavelength passes better through rain showers and causes less sea-echo. For this reason some ships are fitted with a 10 cm as well as a 3 cm radar.

There is a third radar band, the Q-band, with about 8 mm wavelength. Unfortunately this wavelength is not suitable for obtaining a sufficient range owing to excessive attenuation in the atmosphere; the range is limited to about 4 nautical miles.

Linear and circular polarized radio waves

In some radars it is possible to transmit either circular- or linear-polarized radio waves. Reflection depends on the polarization direction; circular-polarized waves give less precipitation-clutter and sometimes also less sea-clutter on the display.

EFFECT OF ATMOSPHERIC CONDITIONS ON RADIATION

It is well known that the rays of the sun are somewhat refracted by the atmosphere towards the Earth. The radiation from radar transmitters undergoes a similar refraction. It is due to the gradual change in refractive index with increasing height, caused by variations in temperature, pressure and humidity of the atmosphere. The refractive index referred to is the ratio of the velocities of the rays in two successive media, the media being layers of air at different temperature, pressure and humidity. The refraction of radar signals under normal conditions is greater than that of light, owing to the much longer wavelengths of the radar waves. This has the effect that *the range of a radar set is greater than the optical range*. The so-called *radar horizon* is located about 6 per cent beyond the optical horizon and about 15 per cent beyond the geometrical horizon. For ships with an aerial height of 20 metres the radar horizon amounts to about 10 nautical miles.

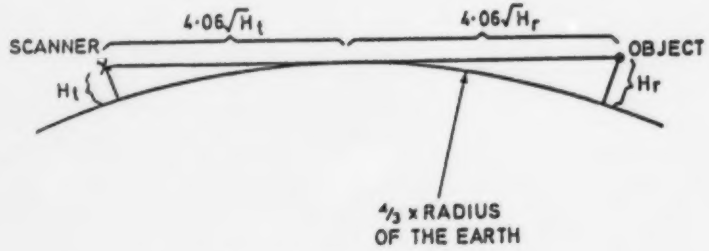


Figure 9.40 Average radar range

Instead of basing calculations on a curved radio-wave path, it is easier to suppose that the radius of the Earth is 4/3 times its actual value; in this case the propagation of 3.2 cm waves may be assumed to follow a straight line. The distance to the radar horizon will then be found more easily (see *Figure 9.40*).

The approximate range may be computed from the formula

$$D = 4.06\sqrt{H_t} + 4.06\sqrt{H_r}$$

where D is the range in kilometres, H_t is the height of the scanner in metres and H_r is the height of the object in metres. It is evident from *Figure 9.40* why the formula is symmetrical in H_t and H_r. The formula has, however, only a limited significance, as it applies only at one specific temperature and pressure at sea level, and assumes a certain decrease of both with height and a certain unchanging relative humidity. The formula is in fact based on the averages of the quantities mentioned for the whole world. Furthermore this formula does not take into account the lobes due to reflection by the sea-surface.

Sub-refraction

Under special atmospheric conditions the refractive index can change so that the radiation is either bent downwards less or even bent upwards. If a diagram is drawn as in *Figure 9.40* with the radius of the Earth assumed to be 4/3 times its actual value, the rays may be bent upwards as shown in an exaggerated way in *Figure 9.41*. This is called *sub-refraction*. It will be seen that the range is now smaller. Sub-refraction may occur at high latitudes, when a cold mass of air flows over a warmer surface (for example, wind blowing over open water after having passed over ice).

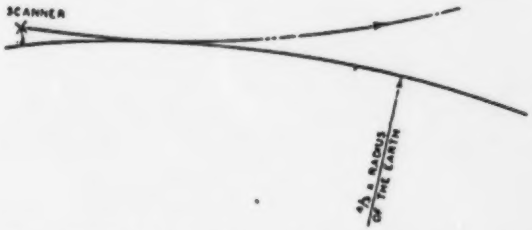


Figure 9.41 Sub-refraction produces shorter radar range

Super-refraction

In *Figure 9.42* the rays are bent downwards more than in a so-called standard atmosphere; this is called *super-refraction*. Super-refraction may occur if the air, after passing over a warm land mass, flows over a relatively cold sea. The greater the temperature difference between air and sea the more this phenomenon will appear. It can thus be expected in the vicinity

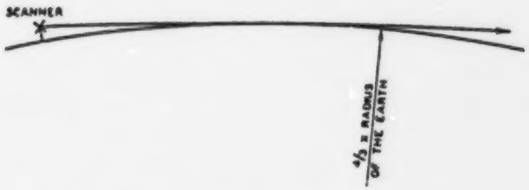


Figure 9.42 Super-refraction produces longer radar range

of land and in temperate and tropical zones. Yet it can also be present on the open sea, far from the coast, especially in the regions of the trade-winds. The effect of super-refraction is that the range may become greater than is normally the case, as is shown by the comparison of *Figures 9.40* and *9.42*.

Super-refraction is encountered quite frequently. In the English Channel, for instance, the wind usually comes from over the land. During the spring and summer, when the land temperature is usually higher than that of the water, super-refraction can be expected during the greater part of every 24-hours. In the Mediterranean, also almost completely surrounded by land, super-refraction has been observed nine days out of ten during the spring and summer.

If the rays are bent down still more, they may be reflected by the surface of the land or the sea, then curved down again, reflected again, and so on (see *Figure 9.43*). This process is called *ducting*, the rays seeming to be confined in a duct. Extremely long ranges of hundreds of nautical miles may occasionally be obtained.

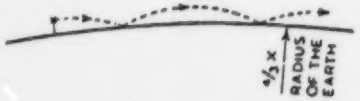


Figure 9.43 Ducting of radar waves

Ducting can also occur at heights of several hundred metres: two adjacent layers of air may have such different refractive indices that the lower layer repeatedly reflects radiation rather than refracting it. In this way a radar transmission or its echo can be propagated a very long distance (sometimes hundreds of nautical miles) before escaping downwards. Apparently inexplicable radar pictures can be brought about, albeit very seldom, by this phenomenon.

Echoes of precipitation and clouds

The water, whether or not frozen, present in the atmosphere as fog, clouds, snow, hail or rain absorbs energy to a greater or lesser degree. This means that some of the transmitter energy and the echo is attenuated, and that objects behind or within an area of mist, clouds or precipitation will produce weaker echoes. Also clouds and precipitation themselves can give echoes that are sufficiently strong to be visible on the screen (*Figure 9.25(a)* and *(c)*). With fog, snow and very light rain this is not the case. If the intensity of the precipitation is sufficient, the echoes on the screen will have the appearance of speckled blots with vague edges resembling wool, and when the echoes are still stronger there is a uniform illumination with well-defined edges. If the edges are vague this helps to distinguish them from land echoes. Sandstorms, which can limit normal visibility drastically, have little effect on radar view. Very heavy sandstorms (wind-force 9), however, show faint uniform echoes which may mask echoes from other ships, etc.

DANGERS OF RADIATION

Radiation from aerial or waveguide

The danger from radiation at very short wavelengths has been investigated very thoroughly by at least three independent groups of experts. After a lot of trials on animals (e.g. mice in waveguides) and measurements of radiation the conclusion may be concisely summarized as follows.

Electromagnetic radiation from the aerial could only be dangerous for a person standing for a long time in the main beam of a non-rotating aerial and at a distance of one metre or less; there the average power can be 10 mW/cm^2. Radiation direct from a waveguide is even more concentrated; when making repairs, for instance, one should avoid standing in front of (and especially looking into) an open waveguide.

At 3 cm wavelength, a sense of heat on the skin surface warns of the presence of radiation. At 10 cm wavelength, a rise in temperature occurs at about 2 cm below the surface of the skin; this is not noticed, and radiation at this wavelength could be dangerous for the eye-lens amongst other things.

Röntgen radiation

It is well-known that when fast-moving electrons hit the screen of a cathode-ray tube (radar or television), Röntgen radiation is produced. The intensity of this radiation is very limited, however. During close investigation both in the United States and in the Netherlands (Royal Navy), no case of permanent injury from this radiation has been found.

Radioactive radiation

Some components (trigatron and T-R switch) exhibit slight radioactive radiation. At a distance of over one foot this radiation is negligible, but one should be careful not to carry parts of these tubes in one's pockets or clothing.

RADAR AS AN AID TO NAVIGATION

To be effective in preventing collisions, it is of the utmost importance that the radar screen should be observed regularly and methodically. It should be borne in mind that new echoes, sometimes at close range, may appear

BUFFER BOARD ECO's
REVISION 2.0

1. Delete capacitor C1 (sheet 1).
2. Delete 1K SIP resistor network RN3 (sheet 2).

CONVERTER BOARD ECO's
REVISION 1.0

1. Cut sides off header shroud of J4 (26-pin conn.) so that it will fit between U101 and U103.
2. Set C10 at 100 pf (sheet 5).
3. Set R18 at 20K ohms (sheet 5).
4. Set R10 at 680 ohms (sheet 1)
5. R4 should be R15 and vice versa (sheet 2)
6. Change U39 to 74LS193 from 74F193 (sheet 3).
7. Set C37 to 10uF tantalum electrolytic. C37 is C52 and vice versa.

DIGITIZER BOARD ECO's
REVISION 1.0

SHEET 2

2.1 Leave out Cap C19, Resistors R36 & R37 and 40 Mhz crystal (Y1).

2.2 Cut signal trace from U10 pin 13.

SHEET 3

3.1 Chip U1, Resistor R4 and Caps C1 & C74 are to be left out since that part of the circuit is now unused. Short R4.

3.2 Short Resistor R5.

3.3 Change Resistor R6 value for 2.0 Kohm.

3.4 Short Resistor R7.

3.5 Change Resistors R8 & R9 values for 2.0 Kohm.

3.6 Change Resistors R16 & R13 values for 2.0 Kohm.

3.7 Change Resistors R12 & R13 values for 10.0 Kohm.

3.8 Change Resistors R10, R11, R14 & R15 values for 2.0 Kohm.

3.9 Change Resistors R25 & R26 values for 2.0 Kohm.

3.10 Change Resistor R27 value for 1.0 Kohm.

3.11 Reverse Diode D2, Cathode to ground, and solder a 100 ohm resistor between pin 1 & 2 of strap E8. Don't jumper E8.

3.12 At Q2, a 2N2906 is used.

APPENDIX I - USERS' COMMENTS

This Appendix includes pictures and reports from the SINADS evaluation onboard the CCGS NICOLET. The reports were prepared by NICOLET's captain, Capt. Sylvain Bertrand and the CCG Navigation Officer, Mr. Richard Michaud. The reports are included in both French and English languages.

OSL would like to thank Capt. Bertrand and Mr. Michaud for their detailed analysis and frank opinions on SINADS. Capt. Bertrand was particularly acute in noting that the system still has a long way to go before becoming a final product: "j'ai réalisé que le projet était encore loin d'un résultat final". As Capt. Bertrand readily understood, OSL submitted a prototype and not a final version of SINADS. Perhaps Mr. Michaud may have lost sight of this fact, but nonetheless, his comments and effort are very much appreciated by OSL. The following paragraphs are OSL's response to Mr. Michaud's and Capt. Bertrand's concerns.

i1. Hardware

Mr. Michaud's comments were most encouraging, for he had nothing but praise for the hardware OSL had selected.

i1.1. Monitor

Mr. Michaud found that the monitor had excellent resolution and an effective anti-glare screen.

i1.2. Keyboard

Mr. Michaud points out the efficacy of directly accessing sub-menus by using the provided menu hard keys on the keyboard. The result is an increase in the speed of commands, for it is now "possible to navigate without having to go through the entire menu as is necessary with PINS".

OSL wishes to stress that the SINADS keyboard has a night-light, but due to oversight it was not displayed during the demonstration. Furthermore, except for the software in lines and stations editing, the numeric key pad works.

i1.3. Computer

Mr. Michaud points out several advantages inherent in using the Motorola computer and UNIX operating system. These advantages include: lower cost of the hardware; operating system security; and communality obtained by programming in standard C. Consequently, as he has noted, SINADS is readily transportable to other vessels with mini computers on board, provided that they have the required processing and RAM capabilities.

i2. Software

Mr. Michaud is more critical of the SINADS software, but it would appear that he has furnished himself with the correct answer: "I feel that the SINADS software in its current form is still in the early stages of development." OSL would like to emphasize again that the system used is a prototype. Not surprisingly, then, as Mr. Michaud points out, many of SINADS options are not operational nor have they been developed to the level of PINS. It must be remembered that PINS has 25 man-years of development, and SINADS has approximately one quarter of that effort.

i3. SINADS vs PINS

Despite the fact that SINADS is still a prototype, Mr. Michaud has, quite correctly, attempted to compare SINADS with PINS. However, OSL believes that any such comparison must attempt to extrapolate into the future a more developed version of SINADS.

i3.1. Access Time

The access time to charts is faster in SINADS, because "all the charts of a given sector, such as the St. Lawrence, [are] digitized in a single block". Furthermore, as Mr. Michaud points out, the "charts need not be loaded into the system memory before they can be displayed, and therefore can be retrieved much more quickly." OSL is pleased that Mr. Michaud has commented on the faster access-time for the charts in SINADS, but wishes to point out that this increase in speed is not a result of digitizing sectors in a single block. Rather, the reason that the charts in SINADS can be loaded faster than in PINS is that the TIN method was used to create them. Moreover, the charts in SINADS correspond to paper charts and not to any single sector block. Thus, unlike PINS, the user in SINADS can call up a chart by merely typing in its Navigation Chart number.

i3.2. Screen Limitations

Mr. Michaud recognizes that "colour and image (resolution) are better on SINADS than on PINS," but he is critical of the display in SINADS, stating that this is where "SINADS has its greatest weakness". His chief criticisms are the limited number of displays and the fact that the operator cannot alter the screen format through the keyboard. This inability, he believes, would limit the adaptability of SINADS to the five Coast Guard regions, which might want to display data differently.

OSL recognizes the justification of Mr. Michaud's criticism of the screen display, and wishes to stress that in this prototype neither the screen layout nor the selection of colour has been fully optimized.

Feedback from current owners of PINS has convinced OSL that most users limit themselves to only one chart display. Thus underlying the creation of the SINADS screen display is the belief that the user is unlikely to want the chart display to be changed except occasionally. Accordingly, OSL plans to provide a number of "pre-designed" screens.

On the other hand, users of SINADS will want to display different types of data as the need arises. Thus unlike PINS, SINADS allows the user to change alpha information in the alpha boxes. By using the hard key ALPHA, the user can quickly enter alphanumerical data in the alpha boxes and can also change the size of the displayed information. For practical reasons, augmentation of the font size is limited to twice its normal size (2X). Thus the font in any alpha box can be reduced/enlarged by its size just by one keypress.

Therefore, by combining a set of pre-designed chart displays with accessibility to alphanumerical display, OSL has attempted to fulfill two objectives: (i) supply maximized graphics and (ii) address the need for displaying both a large amount and a variety of alphanumerical information.

Related to the conceptual differences between PINS and SINADS is the absence of a screen editor in the latter system. Mr. Michaud believes that the lack of a screen-editing function like the one in PINS is a serious flaw, making the user more dependent on OSL. However, as indicated above, feedback from current users of PINS indicates that most users do not modify the screen configuration after the initial set up. Moreover, to change the screen configuration in PINS requires a sophisticated user with sufficient dedication to wade through an Executive Manual that is very demanding to read. Since many vessels are not likely to carry such an individual, the independence from OSL via the use of a screen editor remains at best tenuous. Instead, OSL has produced a simpler method to ensure that even an average user can change the screen configuration in SINADS.

To make the user independent with respect to screen configuration, OSL has designed the SINADS screen layouts in such a way that they can be changed through ASCII configuration files on any ASCII terminal. To accompany the use of the ASCII file, OSL will be producing a Data Processing form that a user will complete by referring to the manual. Filling up the form will only require a copying of numbers, thus removing the need to read a complex Executive Manual. By introducing this method for screen configuration, OSL believes that it will satisfy Mr. Michaud's concern for independence from OSL.

i3.3. Cursor Operation

Mr. Michaud praises SINADS for supplying better cursor control than in PINS because of the addition of in-between keys. He has reservations concerning cursor options, but admits that they do meet minimum requirements. He also criticizes the lack of easy access to cursor function. OSL wishes to point out that SINADS does offer easy access by means of the hard key labelled CURSOR. However, Mr. Michaud's objection to the slow, fixed speed of the cursor is valid. The slowness of the cursor is a recognized bug that will be fixed in the near future.

i3.4. Digital Electronic Charts

Mr. Michaud praises the electronic charts in SINADS, because they have a better screen image with clearly-defined edges rather than "saw-toothed borders," i.e. jaggies. OSL thanks Mr. Michaud for his positive comments, but regrets to point out that the explanation he gives: "SINADS digitalises electronic charts by pixels" is erroneous. Neither PINS nor SINADS digitalises electronic charts by pixels. Rather, PINS uses vector database whereas SINADS uses triangle database or TIN [triangle irregular network]. Moreover, jaggies are a function of screen resolution. While PINS has a resolution of 512 x 380, SINADS has a higher resolution of 1024 x 768. Hence SINADS gives a better image on the screen.

i3.5. Zoom

Mr. Michaud has, with some justification, excoriated the zoom features on the SINADS prototype. He points out that: (1) system operation is lost for a fairly long time, i.e. zoom is too slow; (2) the zoom is fixed to preset values in order to maintain radar capability; and (3) when requesting zoom-in and zoom-out, there is no way of seeing what the chart will look like. He points out that PINS has both a small-scale chart and the outline of a square to indicate what the new chart will look like.

OSL recognizes that the present zoom feature is slow and will be rectifying this problem. Likewise, OSL will be implementing the two features Mr. Michaud liked in

PINS: an outline square and a two-window layout. As to the criticism concerning preset zoom values to maintain radar capability, OSL is at a loss to understand Mr. Michaud's objections. The raison d'être behind the SINADS test was to demonstrate radar equivalence to PPI. Hence the prototype was preset to radar scales. If there were no radar, then zooming could be set to any scale if necessary. However, even with this new-found freedom certain limitations exist. To zoom in too closely is to step beyond the boundary of digitizing accuracy, and this can prove dangerous. To zoom out too far leaves a clutter that would prove of little value to the user.

i3.6. Line and Station Files

As Mr. Michaud has correctly pointed out, neither the line nor the station files are well developed in SINADS. OSL recognizes this limitation in the prototype, and will be rectifying this inadequacy.

i3.7. Station and Line File Management

Again, OSL accepts Mr. Michaud's criticism of the file management system in SINADS as being inadequate. SINADS is designed to have multiple station and line files and file management. However, these have not as yet been implemented in the prototype, but when implemented will meet fully CCG requirements.

In addition, SINADS treats lights, buoys, and all other point features as stations. That is, they are not a part of a chart's database. Consequently, it will be possible to update light and buoy positions, and to include characteristic data associated with both lights and buoys.

i.4. SINADS Radar Image

Both Mr. Michaud and Capt. Bertrand are more critical of the SINADS radar image. Most of their comments relate to the presentation of the SINADS radar image and to its control.

i4.1. Radar Image Presentation

OSL is confused by Mr. Michaud's criticism concerning the radar display in SINADS. Notwithstanding that 80% of the radar distortion was rectified by Mr. Riley, OSL was surprised that Mr. Michaud was not aware that distortion is a limitation produced by the function of radar. On a moving vessel, the image produced is not current because of the two-second rotation.
Furthermore, the NICOLET's radar had to be re-aligned at the beginning of SINADS trials. Yet without a point of reference that a chart supplies, the user remains unaware that normal radar returns are distorted.

Besides mis-alignment, radar returns can often appear ambiguous.Thus the purpose of SINADS is to supply a chart overlay so that radar returns do not merely appear as undifferentiated blips on the screen, but are given a terrestrial context by which they can be defined. Perhaps Mr. Michaud's uncertainty as to the objectives of SINADS led him to state that "it is difficult to justify the use of the RADAR-SINADS system in its current form" since it offers navigators no advantages "except that targets can be visualized on the SINADS screen". A target that can be visualized in a context can be defined.

OSL is also confused by Mr. Michaud's statement that "minute-by-minute update of the digitized radar screen image causes the monitor screen to flicker, making it difficult to work." In fact, the radar update occurs every two seconds and is equivalent to a PPI full rotation. While it is true that SINADS offers a different mode of radar (waterfall as opposed to rotating) OSL hopes that the advantage offered by the display of the targets in a context will far outweigh the force of habit that might make some users reluctant to change. OSL readily admits that SINADS has still a way to go, but it should be understood that it is not offered as a replacement for radar but as an add-on with more features to radar.

Finally, SINADS was developed not only for CCG but for the general-user market. Thus the objective was to allow the system to be interfaced to existing ship radars. Most ships do not carry the expensive ARPA radar. Thus OSL's goal is to offer at a reasonable price a SINADS system that will combine digital ARPa radar capabilities with PINS capabilities.

i4.2. Radar Image Control

OSL recognizes the validity of Captain Bertrand's criticism. As yet, radar controls in SINADS are not fully optimized. The vulnerability of the SINADS radar image to the radar gain control is, unfortunately, a result of the way the Sperry radar functions. In Sperry radars, some processing is performed in the intermediate frequency (IF) section of the transceiver. SINADS uses video signals which are created past the IF section. Most other radars provide raw video that result in the radar gain control not affecting the displayed radar image in SINADS.

i5. Conclusion

OSL thanks both Captain Bertrand and Mr. Michaud for their patience and constructive criticism. OSL will benefit greatly from the thoroughness of their analysis. Furthermore, OSL apologizes for not having elucidated the many underlying concepts such as TIN on which the SINADS prototype is built. Perhaps a fuller explanation by OSL of the goals behind the project might also have prevented some of the misunderstanding that appears in Mr. Michaud's comments. Nevertheless, all the comments were noted, and when the changes are implemented, OSL is confident that it will produce a SINADS system that will prove of great value to the mariner.

SINADS - NICOLET 88

REPORT BY

RICHARD MICHAUD
NAVIGATION OFFICER
LAURENTIAN REGION

NOVEMBER 13, 1988

SINADS SYSTEM

1. HARDWARE

1.1 Monitor

The SINADS system monitor has excellent resolution. Furthermore, the anti-glare screen is very effective and the brightness level need therefore not be raised to maximum in daylight.

1.2 Keyboard

The SINADS keyboard solves one of the problems inherent in the PINS system by providing menu keys through which users can access sub-menus directly. It is also possible to navigate without having to go through the entire menu hierarchy, as is necessary with PINS.

1.3 Computer

The Motorola computer and UNIX operating system provide the following advantages:

(1) Lower cost of main and support hardware, primarily because of lower spare parts costs;

(2) Operating system security, by monitoring users who access the system directly without going through SINADS;

(3) Programming in C, which makes it possible to switch SINADS to other machines; should the Laurentian Region obtain minis for all the ships, SINADS could easily be used on the minis, provided that each system had the required processing and RAM capabilities.

2. SOFTWARE

2.1 Current status

Current status of SINADS software

I feel that the SINADS software in its current form is still in the early stages of development. Why are we bothering with software that has not been developed to the level of PINS? It cannot yet be installed on ships, as the PINS system is. Many of the options are not operational, and those that are have not been developed to PINS level.

3. SINADS VS PINS

3.1 Software

3.1.1 Access time

Access to charts is faster on SINADS, since the system works on a different principle than does PINS; SINADS has all the charts of a given sector, such as the St Lawrence, digitized in a single block. When a chart is retrieved on PINS, the system must access the chart and all the accessory data files. With SINADS, charts need not be loaded into the system memory before they can be displayed, and can therefore be retrieved much more quickly.

3.1.2 Screen image

This is perhaps where SINADS has its greatest weakness. I will grant that colour and image (resolution) are better on SINADS than on PINS, but the problem lies mainly with the display.

SINADS gives a choice of two or three displays, organized along standard lines. The screen is divided into three blocks: (1) position, date and time; (2) direction and speed; (3) NAVLINE data display; (4) STATIONS data display.

The screen format is programmed in and cannot be altered through the keyboard. This means that SINADS cannot be easily adapted to the individual needs of the 5 Coast Guard regions, each of which might require the data to be displayed differently.

PINS provides a screen-editing function, a feature which, in view of possible future changes in Coast

Guard navigation systems, is perhaps the most important. Screen editing allows advanced users to easily change the screen display, for example enlarge part of the display, eliminate unnecessary data, etc. In other words, the user can change the display to meet his current and future needs, without requiring costly software adaptation. The fact that PINS is less dependent on its creators, and that users can adapt PINS to their individual needs without having to go back through OSL, results in greater flexibility and savings of both time and money.

3.1.3 Cursor operation

SINADS

SINADS provides better cursor control, since the keyboard has in-between keys in addition to the normal up-down and left-right keys. This is its only advantage over PINS.

Cursor options are very limited in comparison with PINS, but do meet minimum requirements, which are:

Cursor position
Cursor-ship direction and distance
Cursor-station direction and distance

The cursor position can only be set in relation to the ship's position. It cannot be fixed on the screen as it can with PINS.

With SINADS, cursor speed is fixed, and too slow. PINS users can adjust cursor speed as they wish.

3.1.4 Digital electronic charts

SINADS

SINADS digitalizes electronic charts by pixels, a method which results in a better screen image and more accurate electronic charts. Charts enlarged in scale do not show the saw-toothed border characteristic of vector digitalization and seen in PINS. With pixels, charts retain cleary-defined edges at any scale.

3.1.5 Zoom

The zoom feature on SINADS is dreadful. System operation is lost for a fairly long time; moreover, the zoom is fixed to preset values in order to miantain radar capability. When requesting zoom-in or zoom-out, there is no way of seeing what the chart will look like. PINS outlines a square on the chart which indicates how the new chart will look. This, combined with a small-scale chart on the screen, makes it possible to measure the zoom-out.

3.1.6 Line files

This feature is not well developed in the SINADS system. Course lines can be entered only on the basis of the ship's or the cursor's position. These two modes are unacceptable when dealing with a river course, since we must be able to enter the exact co-ordinates for a given course using the keyboard. Even though PINS has this capability, the feature is not very effective since the digital keyboard offered with BARCO (the PINS monitor) cannot be used.

Moreover, courses cannot be plotted with SINADS as they can with PINS; PINS allows courses to be plotted using NODES, a feature which greatly increases the flexibility of this option.

3.1.7 Station files

Station operation

SINADS and PINS are very similar; however, as before, digital data entry is only possible using PINS.

3.1.8 Station and line file management

Both SINADS and PINS have extremely unsatisfactory file management systems. Each chart should have all its course and station files assigned to it. However, all SINADS can do is call up all the files onto the screen, while PINS does not even hold a list of files.

With the current PINS system, the production of course and station files is not very popular with users, since the software is badly organized and a digital keyboard can be used to enter data.

SINADS will cause the same problems; perhaps worse, users will ignore this feature altogether, since too many operations are required and the procedure is not clear.

Moreover, if cursor movement on the SINADS system is not improved, the NAVLINE and STATION options will suffer as a result of cursor control problems.

3.2 SINADS VS PINS
COMPARISON IN TABLE FORM

OPTION OR CHARACTERISTIC	SINADS	PINS
Screen		
General characteristics	Excellent	Good
Definition	Superior	Poor
Colour	Better	Adequate

OPTION OR CHARACTERISTIC	SINADS	PINS
Keyboard		
General characteristics	Very good	Adequate
Night lighting	No	No
Access to digital pad	No	No
Choice of computer: Significance for user	Smaller size	
Cursor		
Speed	Fixed	Adjustable
Ship cursor	Yes	Yes
Station cursor	Yes	Yes
Position cursor	Yes	Yes
Easy access to cursor function change	No	Yes
Screen editing and mode change capability	OSL only	Available
Font change	OSL only	Available
Addition of extra screen	OSL only	Available
2- or 3-chart display	OSL only	Available
Zoom		
Speed	Too slow	Adequate
Visualization	Radar distance	Multiple scales
Radar	Yes	No

4. RADAR-SINADS OPTION

The RADAR-SINADS option is still in the early stages of development. The feature will have to be much improved before navigators can use it on a monitor.

As the system is now, the radar image on the monitor screen is distorted and does not have the same reference points as its equivalent on the radar screen. The minute-by-minute update of the digitized radar screen image causes the monitor screen to flicker, making it difficult to work. Navigators do not like the system, as it forces officers to change the way they work.

It is difficult to justify the use of the RADAR-SINADS system in its current form, since navigators have found that it offers no advantages (except that targets can be visualized on the SINADS screen) and is not as highly developed as PINS. Radar continues to be the tool of choice for the IMO and Coast Guard Ship Safety.

The fact that system development was based on the old Sperry MK127 technology, when the Laurier has already been fitted with digital ArpA radar, and the rest of the fleet is soon to follow, demonstrates considerable lack of foresight.

CONCLUSION

This report expresses my personal opinions and do not necessarily reflect those of management.

(signed)
Richard Michaud
Navigation Officer
Laurentian Region

SINADS - NICOLET 88

RAPPORT
PRODUIT
PAR

RICHARD MICHAUD
OFFICIER DE NAVIGATION
REGION DES LAURENTIDES
15 NOVEMBRE 1988

SYSTEME "SINADS"

1. MATERIEL INFORMATIQUE

1.1. ECRAN

L'image offerte par le système "Sinads" est d'une excellente résolution. De plus l'écran anti-reflet est très efficace et ne requiert pas que l'intensité soit montée au maximum en plein jour.

1.2. CLAVIER

Le clavier règle un des problèmes qu'on a eu dans l'implantation du système "PINS", grâce un clavier avec dés touches de menus définies, l'usager du Sinads a accès aux sous-menus en pesant sur une touche et de plus peux naviguer sans être obligé de remonter la hiérarchie des menus comme dans le PINS.

1.3. ORDINATEUR

Le choix de l'ordinateur Motorola et du système d'exploitation UNIX, permet

1 - Un coût moins élevé pour le matériel informatique de soutien et principal soit les pièces de rechange principalement.

2 - Une sécurité au niveau du système d'exploitation soit le contrôle des usagers accédant au système direct sans passé par SINADS.

3- La programmation en C permet la portabilité du système SINADS sur d'autres machines. Si la région des Laurentides se procure des minis pour chaque navire, ces systèmes pourraient facilement être utilisés pour SINADS moyennant que les besoins en traitement et mémoire RAM soit rencontré par le système en question.

2. LOGICIEL

2.1. ETAT PRESENT

Etat présent du Logiciel "SINADS"

Le logiciel dans sa présente forme est dans un état de développement très peu développé selon mon point de vue. Pourquoi ? ce ramasse-t-on avec un logiciel dont le niveau de développement n'atteint pas le niveau du PINS. Le logiciel présentement ne peut être appliqué sur un navire au même le PINS l'est. Beaucoup des options ne sont pas opérationnelles, de plus celles qui le sont, n'ont pas été développer au niveau du PINS.

3. SINADS VERSUS PINS

3.1. LOGICIEL

3.1.1. TEMPS D'ACCES

TEMPS D'ACCES

Les temps d'accès sur Sinads sont diminués pour les cartes car le principe n'est pas le même que le PINS, le SINADS a toutes les cartes d'un secteur comme le fleuve numéralisé en un bloc. Lorsque vous appelez un configuration ou une carte celle-ci n'a pas besoin d'être charger en mémoire mais plutôt ses accessoires ce qui prend beaucoup moins de temps à charger que le PINS.

3.1.2. PRESENTATION VIDEO

La Présentation Vidéo

C'est peut-être où SINADS faillit le plus, je suis d'accord sur le fait que les couleurs et l'image (résolution) est meilleur sur le SINADS que sur le PINS, mais c'est surtout sur le mode de présentation.

Avec SINADS, vous avez le choix de 2 ou 3 affichages, de plus ces affichages sont organisés de manière très standard. L'écran est organisé en bloc: 1- Position, date,temps 2 -Direction, vitesse 3- Affichage des données sur les NAVLINE 4- Affichage des données sur les STATIONS.

Ces écrans font partie de la programmation, il ne sont pas accessible par le clavier pour une refonte, ce qui rend SINADS très peu adaptable aux besoins multiples de la Garde Côtière car vous avez 5 régions donc 5 manières de visualiser et d'utiliser l'information présentée.

Ce que PINS possède et est peut-être la capacité d'adaptation la plus importante du système pour les changements futurs des systèmes de navigation à la Garde

Côtière, c'est son mode d'édition d'écran où un usager avancé peut facilement changer la présentation à l'écran, soit grossir des informations, garder l'essentiel, etc.. En bref permettre à l'usager de rencontrer ces besoins en information présents et futurs sans être obligé de demander une modification très coûteuse au logiciel. Le fait que les usagers peuvent adapter PINS à leur besoin sans passer par OSL, permet une meilleur flexibilité et une économie de temps et d'argent due à l'indépendance du PINS versus ses concepteurs.

3.1.3. OPERATIONS DU POINTEUR

LE POINTEUR

SINADS

On a un meilleur contrôle sur le pointeur à cause du clavier qui n'offre pas seulement les touches nord-sud et est-ouest mais aussi les intermédiaires. Autrement c'est la seul qualité par rapport au PINS.

Les options d'opérations pour le pointeur comparativement au PINS sont très limitées mais rencontre le minimum soit:

Position du pointeur
Direction distance pointeur-navire
Direction distance pointeur-station

On ne peut utiliser le pointeur qu'en mode relatif au navire, sur PINS on pouvait le mettre stable à l'écran.

La vitesse de déplacement du pointeur est fixe sur SINADS et par surcroit trop lente. Sur PINS l'ajustement de la vitesse était au goût et au besoin de l'usager.

3.1.4. CARTES NUMERIQUES

SINADS

Sinads utilise la numéralisation par pixels, ce qui a pour effet d'avoir une meilleure présentation à l'écran et une meilleur précision des cartes. Lorsque vous grossissez l'échelle de la carte vous n'avez plus les bords en dents de scie, caractéristique propre au système à numéralisation vectorielle comme le PINS. Par pixels, vous obtenez un image dont les contours de la carte reste bien définie sur toutes les échelles.

3.1.5. ZOOM

LE ZOOM

Sur SINADS, cette fonction est détestable car on perd l'opération du système pour une assez bonne durée, de plus le zoom est fixe selon les valeurs préétablies pour être capable de faire fonctionner le radar. On ne voit pas lorsque l'on demande le "zoom-in" ou "zoom-out" de quoi devrait ressembler la carte. Sur PINS il y a un carré qui vient se placer sur la carte pour indiquer comment devrait se présenter la nouvelle carte de plus avec une carte de petite échelle à l'écran, cela nous permet de mesurer pour un "zoom-out".

3.1.6. OPERATIONS DES LIGNES DE NAVIGATION (LINES FILE)

OPERATIONS DES LIGNES DE NAVIGATION

Présentement avec SINADS l'option est très peu développé, on ne peut entrer des lignes de navigations que par soit la position du navire ou par la position du curseur. L'entrée dans ces 2 modes pour un navigateur de rivières est inacceptable car il faut être capable d'entrer les coordonnées parfaites d'une ligne par voie du clavier. PINS le fait mais très mal car on ne peut se servir du clavier numérique déjà offert sur le BARCO (moniteur utilisé sur le PINS).

De plus sur Sinads la production de lignes ne se fait pas comme avec PINS où l'on peut utiliser des NODES pour faire les lignes ce qui rend encore une fois l'accès à cette option beaucoup plus souple.

3.1.7. OPERATIONS DES STATIONS (STATION FILE)

OPERATIONS DES STATIONS

SINADS et PINS se ressemblent beaucoup sauf encore une fois l'entrée numérique n'est possible que sur PINS.

3.1.8. GESTION DES FICHIERS DE LIGNES ET DE STATIONS

GESTION DES FICHIERS DE LIGNES ET DE STATIONS

SINADS et PINS sont tous les deux des enfants pauvres sur cette facette de l'application. Chaque configuration ou carte doit avoir assigner à celle-ci son ensemble de fichiers de lignes ou stations qui lui sont propre. Hors SINADS ne fait que rappeler à l'écran tous les fichiers, PINS n'a même pas de liste de fichiers.
Présentement sur PINS, la production de fichiers de lignes et de stations n'est pas populaire au niveau des usagers à cause du manque d'organisation au niveau du logiciel et le fait de pouvoir opérer un clavier numérique pour l'entrée de données.
La même chose va se produire sur SINADS et même pire, ces option vont probablement être laisser carrément de coté par les usagers due au fait qu'ils requièrent trop de manipulation et le traitement n'est pas évident.

De plus sur SINADS si le pointeur demeure dans son état actuel de capacité de mouvement, les options NAVLINE et STATIONS du logiciel vont en souffrir à cause des_ problèmes de manipulation du pointeur.

3.2 TABLEAU COMPARATIF SINADS VERSUS PINS

OPTIONS OU QUALITES	SINADS	PINS
ECRAN- QUALITES GENE.	EXCELLENTE	BON
DEFINITION	SUPERIEUR	FAIBLE
COULEURS	MEILLEURES	PASSABLE

[illegible] – [illegible]

OPTIONS OU QUALITES	SINDOS	PINS
CLAVIER- QUALITES	TRES BON	PASSABLE
ECLAIRAGE NUIT	NON	NON
ACCES AU PAD NUMERIQUE..................................	NON	NON
IMPORTANCE DE CHOIX DE L'ORDINATEUR POUR L'USAGER...........................	MOINS VOLUMINEUX	....
POINTEUR		
REGLAGE VITESSE	AUCUN	AJUSTABLE
POINTEUR-NAVIRE	OUI	OUI
POINTEUR-STATION	OUI	OUI
POINTEUR POSITION	OUI	OUI
ACCES FACILE AU CHANGEMENT DE FONCTIONS DU POINTEUR............................	NON	OUI
EDITION D'ECRAN ET CHANGEMENT D'UTILISATIONS......	OSL SEULEMENT	DISPONIBLE
CHANGEMENT DE LETTRAGE	OSL SEULEMENT	DISPONIBLE
ADDITION D'UN NOUVEL ECRAN................................	OSL SEULEMENT	DISPONIBLE
VUE AVEC 2 OU 3 CARTES.....	OSL SEULEMENT	DISPONIBLE
ZOOM		
VITESSE	TROP LENT	ACCEPTABLE
VISUALISATION	DISTANCE RADAR	ECHELLES MULTIPLE
RADAR	OUI	NON

4.0 L'OPTION RADAR - SINADS

L'option RADAR-SINADS, présentement l'option radar est à son développement initial, il reste beaucoup à développer afin qu'un officier de navigation puisse utiliser une telle option sur un moniteur.

Dans son état actuel, l'image radar qui apparait sur le moniteur est distorsionné et ne possède pas les mêmes valeurs de relèvements que sur le radar. Le fait que l'écran radar numéralisé est rafraichi toutes les minutes, provoque des sauts à l'écran du moniteur, rendant difficile le travail et n'obtient pas un vote de confiance par les navigateurs car ceci change le mode de travail des officiers.

Avec la présentation actuelle, il est difficile de savoir à quoi cela va mener car le système SINADS avec radar n'offre aucun avantage à l'exception de visualiser les cibles sur l'écran Sinads, n'est pas développé au niveau du PINS, et du point de vue des navigateurs. Un radar reste l'outil encore reconnu auprès de l'OMI ou le Service d'inspection des Navires de la Garde Côtière.

Le fait de développer sur de la vieille technologie Sperry MK127 alors que la flotte possède déjà des radars numériques ArpA sur le Laurier, ceci est un manque de prévoyance car la flotte va changé ces vieux radars dans un avenir rapproché.

CONCLUSION

Ce rapport demeure mon opinion personnel et n'engage en rien la gestion

Richard Michaud

Richard Michaud
Officier de navigation
Région des Laurentides

MEMORANDUM

To: Captain Raymond D'Amours
DFMB

From: Sylvain Bertrand
Captain
CCGS Nicolet

Date: 14-11-88

Subject: SINADS system report

Below are some of my views on the SINADS system, as requested.

At first, I was very interested in the idea of combining a radar image with a digital map.

After a few days, I realized that the project still has a long way to go before it is truly viable.

1. Distorted radar image

   In the first three weeks, we noted that there was distortion between the polar projection and the UTM map, sometimes by as much as 300 feet. Mike Reley, a specialist from Montreal, eliminated some 80% of the distortion, although some remained at the corners of the screen.

2. Radar image lag

   In addition to the Doppler shift, which we expected to have some effect, we noted that the radar image is too far forward in front of the ship and lags behind the ship. This may be detected by observing the buoys. This is a major problem, which is caused by the two-second lag in transposing the radar data after each complete sweep of the antenna, and which could be resolved only by processing the radar data and transposing it to the monitor screen immediately. With a ship like the Radisson coming down the Richelieu river at 16 knots with a 5-knot downstream current, the position shift in the two-second lag is considerable.

(ANNEX 1 - CONT'D)

3. Radar image control

The radar image on the SINADS screen is far too vulnerable to the radar controls, particularly to the gain control. Use of the gain control to detect echos on the radar screen directly affects the radar image on the SINADS screen, either causing part of it to disappear or amplifying echos to the point where nothing can be seen on the screen at all.

Morover, I find that the image precision on the radar screen is adversely affected when transposed onto the SINADS screen; echo returns are lost and the final adjustment is not equivalent to that on the radar screen. The SINADS image must therefore be adjusted constantly whenever the ship is sailing in poor weather or through ice. That adjustment is made even more difficult by the two-second lag. It takes up too much of the officer's time.

4. Azimuth clutter

With a short-range image, a sun takes up the centre of the image. To make it disappear, the Azimuth Clutter control must be pressed. However, when the range is increased, the screen fills with false echos, requiring yet more adjustments which should not be necessary.

5. Edge control

This does not give the expected results. Lines should be made more distinct in order to show the coastline clearly and reduce the rest of the echos; however, when this feature is switched on the entire image is damped with no change in contrast.

6. SINADS/PINS

For a comparison of the two systems, I have attached the report prepared by Richard Michaud, which includes some of my comments.

On the whole, I would say that I still consider this to be a very good idea, but I feel that the system needs to be further refined.

Sylvain Bertrand
Captain
CCGS Nicolet

Government of Canada
Gouvernement du Canada

MEMORANDUM NOTE DE SERVICE

CAPITAINE RAYMOND D'AMOURS
DMFB

SYLVAIN BERTRAND
COMMANDANT
NGCC NICOLET

SECURITY - CLASSIFICATION - DE SECURITE

OUR FILE/NOTRE RÉFÉRENCE

YOUR FILE/VOTRE RÉFÉRENCE

DATE 14-11-88

SUBJECT
OBJET **RAPPORT SYSTEME " SINADS "**

Tel que demandé, voici quelques observations sur le système "SINADS"

A prime abord, l'idée de combiner une image radar au dessus d'une carte digitalisée a soulevé de beaucoup mon intérêt.

Dès les premières journées, j'ai réalisé que le projet était encore loin d'un résultat final.

1- Image Radar distorsionnée.

Les 3 premières semaines, on remarquait des distorsions entre la projection polaire du Radar et celle de la carte UTM pouvant aller jusqu'à 300 pieds. Un spécialiste de Montréal M. Mike Reley a résolu le problème de 80%. Il reste tout de même encore une distorsion surtout aux extrémités inter-cardinal de l'écran.

2- Retard image Radar 9

En plus de l'effet DOPPLER qui doit affecter un peu, on remarque que l'image Radar est en avance sur la carte en avant du Navire et en retard en arrière du Navire. On s'apperçoit de ce phénomène en observant les bouées. Ce gros problème provient du 2 seconde de délai sur la transposition de l'information Radar après un balayage complet de l'antenne. Pour résoudre ce problème, l'information recueillie de l'antenne devrait être traitée et envoyée immédiatement à l'écran. Pour un navire tel le Radisson qui descend à 16 noeuds dans le " Richelieu " avec un courant baissant de 5 noeuds, on pourrait observer un très grand décallage de transposition à chaque 2 secondes.

(SUITE ANNEXE 1)

(ANNEXE 1 SUITE)

3- Contrôle image Radar

Limage Radar sur l'écran " SINADS " est beaucoup trop vulnérable aux contrôles du Radar, spécialement le gain. Lorsqu'un officier manipule cette commande pour déceler des échos sur le Radar, il affecte directement l'image Radar du SINADS soit en enlevant en partie l'image ou en augmentant le retour des échos de façon à ne plus rien voir sur l'écran.
De plus, je trouve que la précision de l'image Radar est affectée lorsqu'elle est transposée sur l'écran SINADS, on perd des retours d'échos et l'ajustement final n'égal pas celui du Radar lui-même. Par conséquent, le système SINADS est sujet à de constants ajustements lorsque le navire navigue soit par mauvais temps ou dans les glaces et cet ajustement est d'autant plus difficile à obtenir du au délai de 2 secondes. Il monopolise l'officier trop longtemps.

4- Azimut CLutter

Par petite portée, un soleil occupe le centre de l'image,pour le faire disparaitre on presse la commande Azimut Clutter, mais lorsque l'on augmente la portée, l'écran se rempli de faux échos, ce qui demande encore des ajustements non justifiés.

5- Contrôle EDGE

Ne donne pas le résultat escompté. Une ligne devrait apparaître plus clairement pour mettre en valeur le contour de la côte et amoindrir le reste des échos mais avec ce contrôle en opération le tout est diminué sans différence.

6- SINADS/PINS

Pour la comparaison des deux logiciels, je joins le rapport de M. Richard Michaud qui inclus mes commentaires.

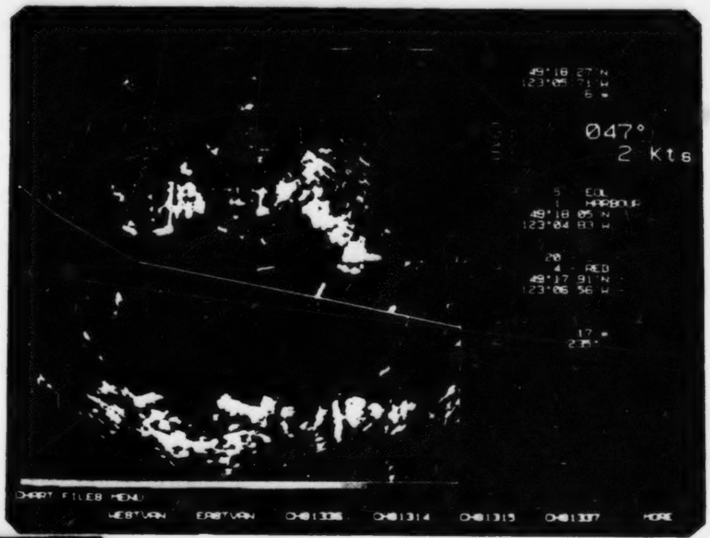
Pour terminer, je considère que l'idée est toujours bonne mais devrait avoir une précision plus accrue.

SYLVAIN BERTRAND
COMMANDANT
NGCC NICOLET

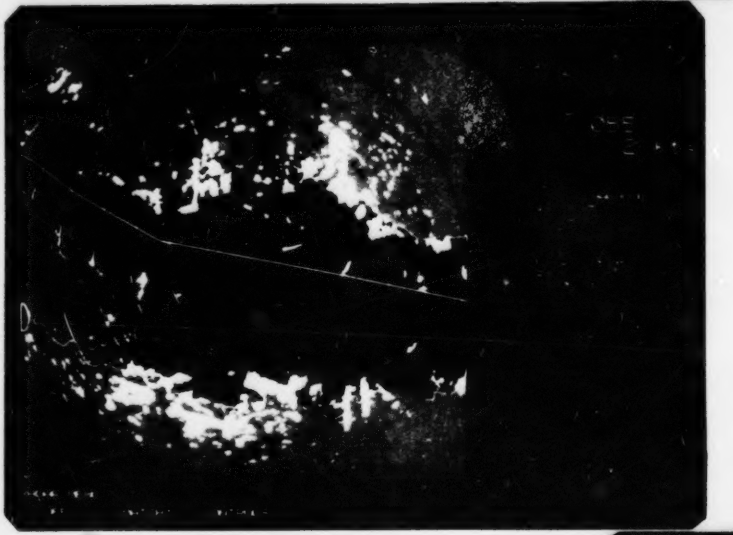
SB/PL

p.j.

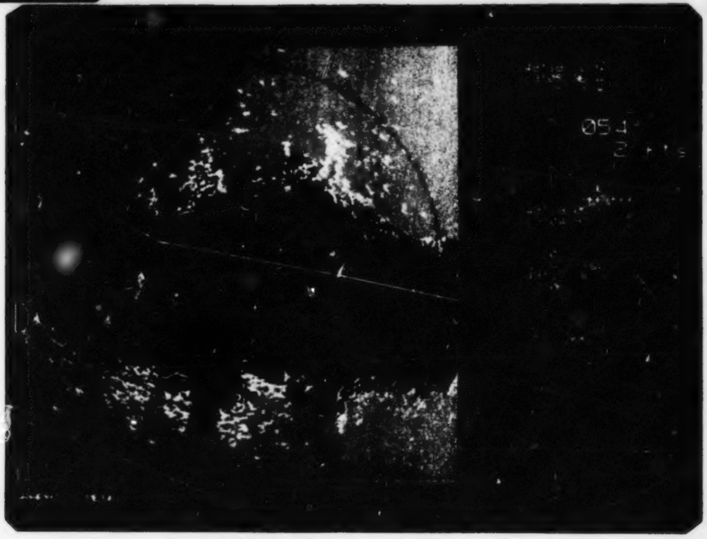
SINADS


49°18 27 N
123°05 71 W
6
047°
2 Kts
5 EOL
1 HARBOUR
49°18 05 N
123°04 83 W
20
4 RED
49°17 91 N
123°06 56 W
17
235°
CHART FILES MENU
WESTVAN
EASTVAN
MORE

RADAR IMAGE with
ROUTE GRAPHICS of
Vancouver Harbour



ELECTRONIC CHART with
RADAR IMAGE OVERLAY

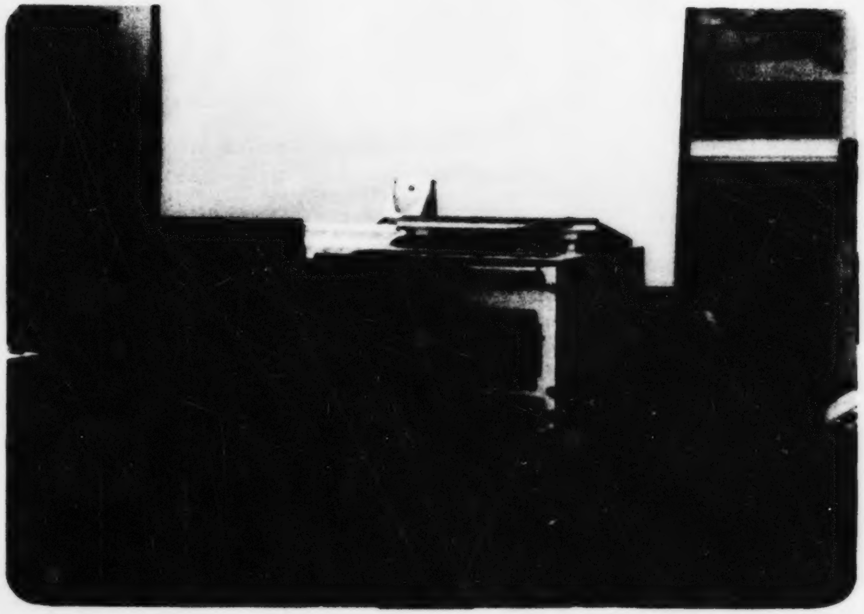


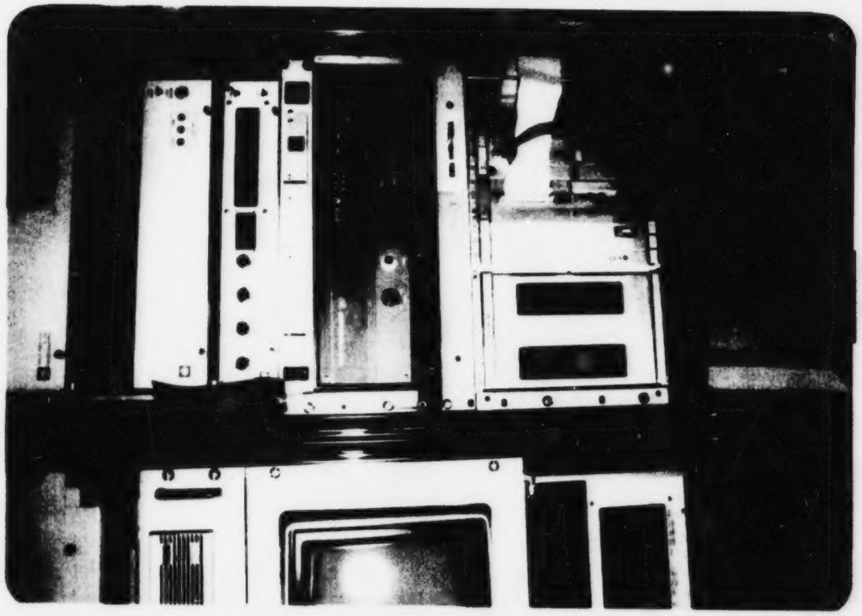
ELECTRONIC CHART with
EDGE ENHANCED RADAR IMAGE
for Ship Positioning

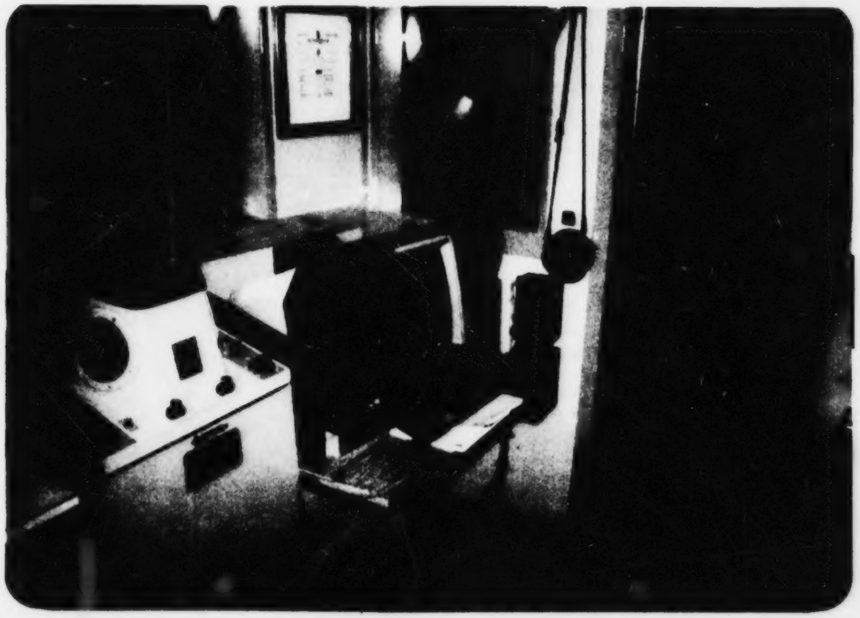
CCGS NICOLET used as a test platform for the SINADS trials in the St. Lawrence River.

Brigde of the CCGS NICOLET

Electronics Room of the CCGS NICOLET located behind the bridge



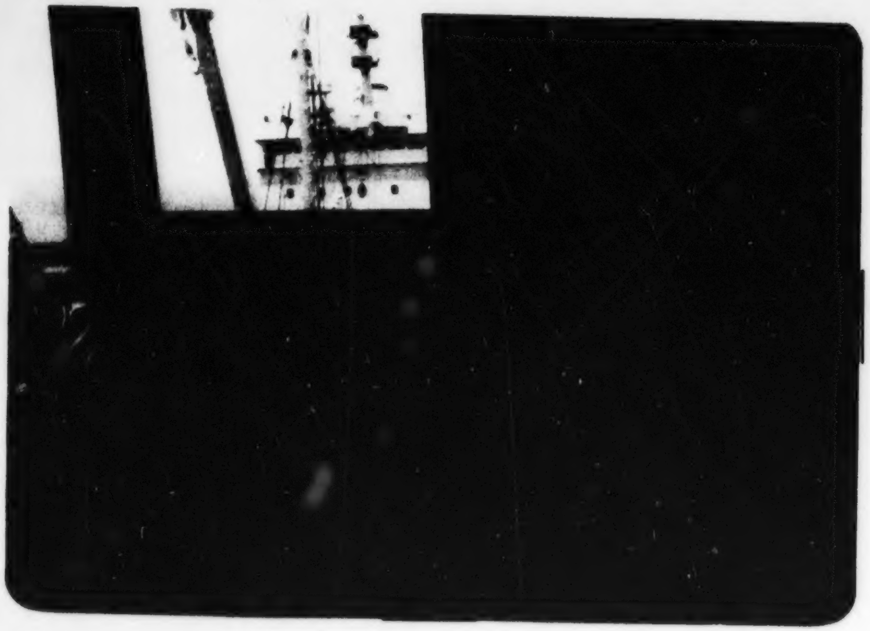


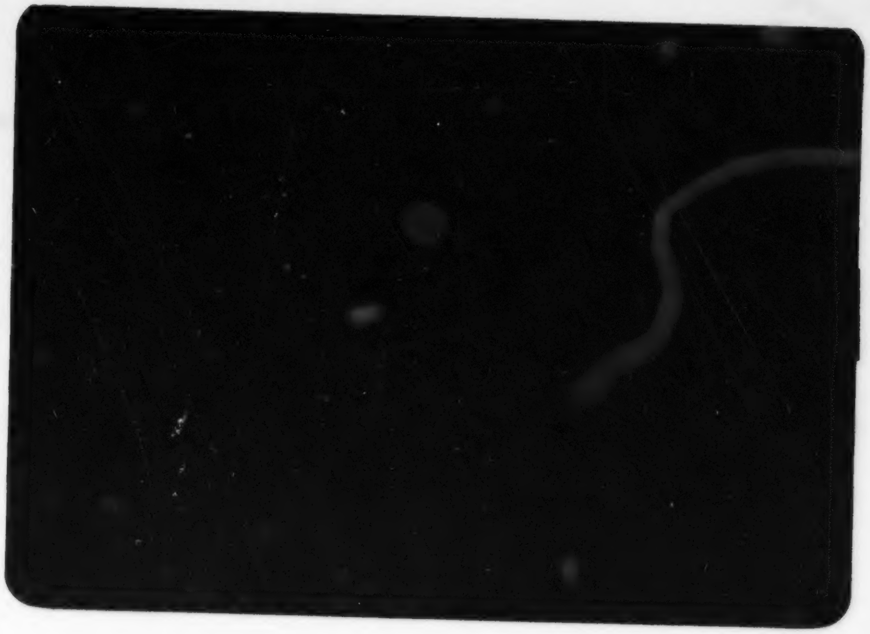


SINADS simulator
(from the left: 14" monitor, Computing
System, positioning simulator display)

SINADS hardware used during the
trials (from the top: Computing System,
Mini-Ranger console, OSL gyro interface)

SINADS Interactive Display Console
located on the bridge beside the radar PPI





SINADS Interactive Display Console
visible in the daylight conditions.

Chart of the Quebec City with
overlayed radar image and compass rose

Chart of the Quebec City with
overlayed radar image and
radar range rings

APPENDIX J - OPERATIONAL REQUIREMENTS

The requirements for an operational SINADS are described in the following paragraphs.

j1. Precise Vessel Positioning

The difficult manoeuvering operations in narrow channels or at berth require that the navigator is provided with the real-time precise (±3 metres) positioning information. To simplify the interpretation, this information should be presented in a graphical form showing the scaled ship outline on the electronic chart. The indication of the position error should be also provided in form of an error ellipse. A number of alarms should allow the user to monitor distances from known point-of-danger like shallow water, docks, buoys, etc.

j2. General Inshore Navigation

The general requirement within the marine industry calls for a standard bridge console which would constantly update ship's position (±20 metres) on an electronic chart. The comparison of the radar imagery to the shore outline should verify the ship's position. The interpretation of the radar image should be simplified and the objects in the water should be highly visible. The system should also provide the collision-avoidance and route-planning capabilities.

j3. Open-Ocean Navigation

The standard bridge console could also be used for open ocean navigation (±200 metres). The console should allow the integration of all ship's sensors on one display. The interface to the Maritime Integrated Navigation System (MINS) developed by the Canadian Navy, could provide a graphical display which this open-ocean navigation system is currently lacking.

j4. CCG Search and Rescue (SAR) operations

The search and rescue operations require a system which would provide a combination of the precise positioning, search planning and target tracking capabilities. The system should be capable of piloting the rescue vessel navigator along the search-pattern-lines and should clearly display the radar contacts in the water as well as the land radar image aligned with the electronic chart.

j5. CCG Vessel Traffic Services (VTS) Operations

The stationary application of a vessel traffic management system requires a combination of the local chart display, one or two radar overlays, target tracking capabilities, and a vessel database. All that information combined on a single monitor should provide a real-time display of the harbour traffic and the current location of shipping.

j6. Naval Shipboard Navigation And Tactical Displays

The tactical operations require an integrated console in the Operations Room. Such console should integrate all navigational inputs and combine on one screen the electronic chart, radar imagery and tracking capabilities for both surface, airborne and subsurface targets. This can be achieved by interfacing to a variety of tracking systems and by integration of all navigational and tactical information on one single command and control system console.

j7. Naval Mine Countermeasures Operations

The mine countermeasures operation requires a system which could combine navigational function with route-survey and mine-hunting capabilities. The interface to a side-scan-sonar system, acoustic positioning system and cable winch can provide all information necessary for an effective route-survey system. The routes and survey grids should be stored in advance in the memory and the positions of sonar contacts should be added to an electronic chart. The interface to an ROV or sweep-gear positioning systems can provide graphical display for these operations.

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